**Template for Faculty Data**

**Faculty Name Tarni Joshi**

Designation: ASSISTANT PROFESSOR (CONTRACT)

Employee ID: 3305119

Qualification: M.TECH

Phone No.: NIL

Email Id: tarnijoshi88@gmail.com

1. 
2. **About Faculty**

I am leaning toward the depth of VLSI analog or digital design. Furthermore, I am highly interested enhance my strive to create a challenging and engaging learning environment. Notable track record of education & research success with multiple published articles.

Core Competencies:- VLSI Technology, CMOS VLSI Design (circuits & system), Microprocessor & Microcontroller, Digital Electronics, Embedded system & RTO’s, Fundamentals of Measurement system, Transducers, Intelligent Instrumentation, Basic Electronics, Communication and Presentation Skills.

1. **Educational Qualification (As given in biodata uploaded on website)**

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| --- | --- | --- | --- | --- |
| S. No. | Degree | Specialization | Year | University/Board |
| 1 | M.Tech | VLSI Design & Embedded System | 2014 | RGPV, Bhopal |

1. **Work Experience**

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| --- | --- | --- | --- | --- |
| S. No. | Designation | Department | Employer Name | Duration of Employment |
| 1. | Asst. Prof. (Contract) | Elex. & Instrumentation Engg. | Tarni Joshi | 3.5 years |

1. **Research Detail**

* Project Title : Design and Analysis of Current Starved VCO for RF applications (M.tech )
* My Role : Designing, Implementation, Synthesis & Analyze Tool/Platform Used : Tanner EDA Tool
* Description : This research work will provide a study for the Current Starved VCO and its utility in the field of PLL. It will also give the details for using the Current Starved Topology in Ring VCO. The project will govern on Tanner 70nm technology.

1. **PhD Supervision:-** Nil
2. **Publication**

* International paper published in International Journal of Engineering Sciences & Research T echnology, IJESRTon “Current Starved VCO designed using 70nm CMOS Process” IJESRT 5(3), March 2016.
* Presented & published paper at National Conference held Sanghvi Institute of management & Sciences Indore on 28-29 Sept 2012 sponsored by AICTE & IEEE on the topic “ Review on Performances: Current Starved VCO Using 0.18um CMOS Process”
* Presented & paper published paper at National Conference held Sanghvi Institute of management & Sciences Indore on 28-29 Sept 2012 sponsored by AICTE & IEEE on the topic “ High Performance CMOS LC VCO-A Review”International paper published in IJEATE on “ Architectural Review: Evolution of Embedded Digital Signal Processors” Issue April, 2012 volume I.
* Presented and published paper at National Conference held at Gyan-Ganga College of science & technology, Jabalpur on 2-3 March 2012 sponsored by AICTE & MIPS.

1. **Project :- Nil**
2. **Testing & Consultancy:-Nil**
3. **Other Details**

* **Workshop Attended**
* Attended Faculty Development Programme organized and conducted by Teaching Learning Centre IIT-Madras from 4thto 8th June 2018.
* Attend 2-week (30thJan to 4thFeb 2017) ISTE-STTP Workshop on “CMOS, Mixed signal & Radio Frequency VLSI Design” conducted by IIT, Kharagpur under the National on Education through ICT (MHRD)
* Attended 4 days (26thDec to 29thDec 2016) Workshop on “ Vendor training program on Mentor Graphics EDA Tool” conducted by Electronics & Instrumentation Dept., Shri G.S. Institute of Technology & Science, Indore (M.P.)
* Attend 5 days (30th Aug’16 to 3rd Sept’16) workshop on “Training on Advanced Instrumentation methods” conducted by M.P. Council of Science & Technology, Bhopal under Quality Assurance Laboratory programs.
* Training Experience
* Instrumentation, system & Automation Society (ISA), Pune (6 days – Feb’2009)
* Training in PLC’s (Allen Bradley, Siemens, Mitsubishi, Messung, MMI, SCADA Drivers & LEC standards programming)
* Bhilai Steel Plant, SAIL, Bhilai (3 week – 30thJune to 19 July 2008) Vocational Minor training under department of Instrumentation
* Bhilai Steel Plant, SAIL, Bhilai (3 week – 6thJuly to 25thJuly 2009)
* Major training and 3 week project based training at BSP, Bhilai.
* Responsibilities handled:
* Worked as member of organizing committee in five day STC on RECENT TRENDS IN VLSI DESIGN from 09-13thApril 2018, sponsored by TEQIP-III at Electronics & Instrumentation Dept. SGSITS Indore.
* Worked as a Co-Conveyer in Electronics & Instrumentation departmental technical event held under annual fest AAYAAM-2018 at SGSITS Indore.
* Worked as member in certificate & prizes distribution committee in annual fest AAYAAM-2017 organized at SGSITS, Indore.