Shri G. S. Institute of Technology and Science

Department of Electronics and Instrumentation Engineering

Four Week Internship

on

Analog Chip Design

Celebrating 72 Year

PRESENTED BY

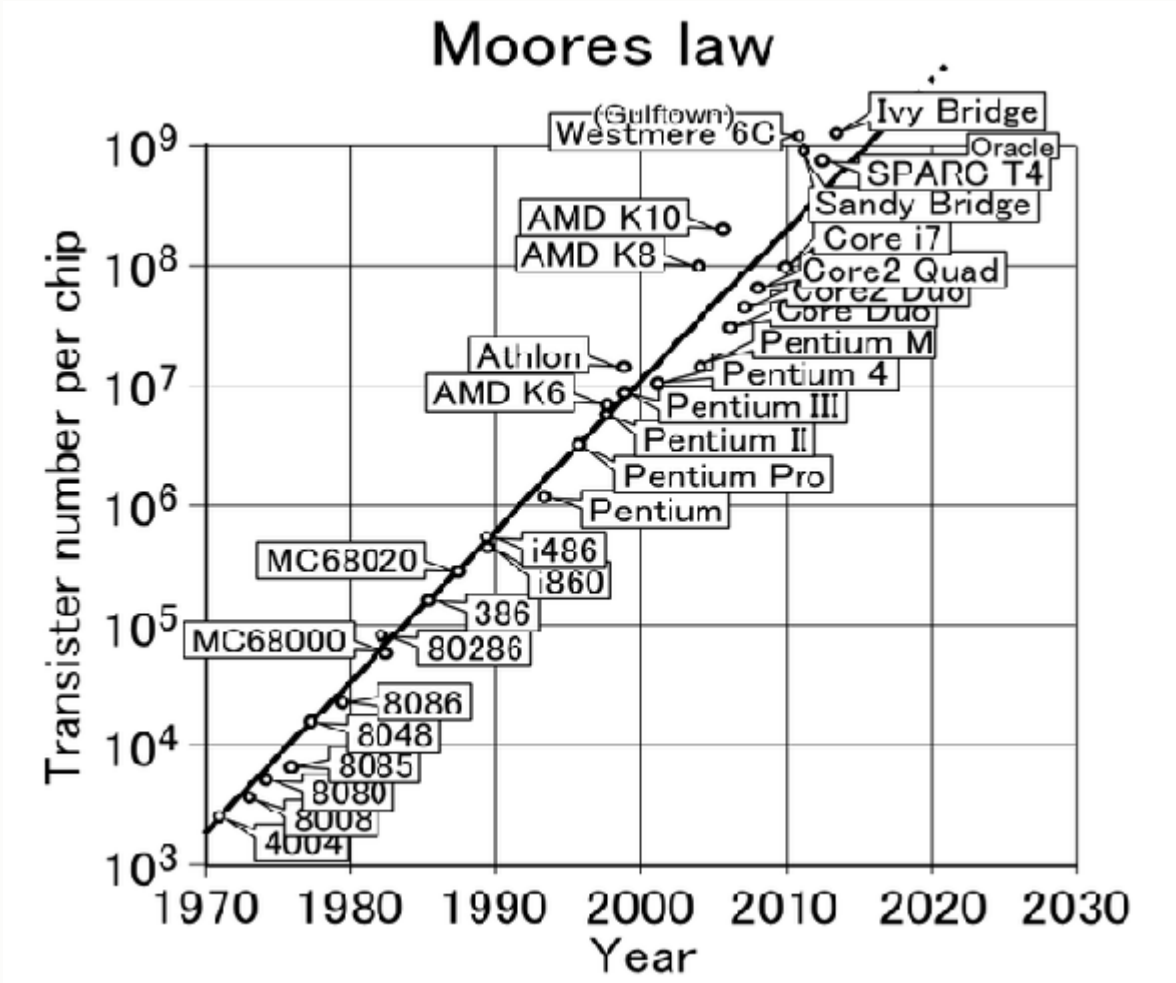
Dr. Rajesh Khatri (Associate Professor)

Analog Chip Design

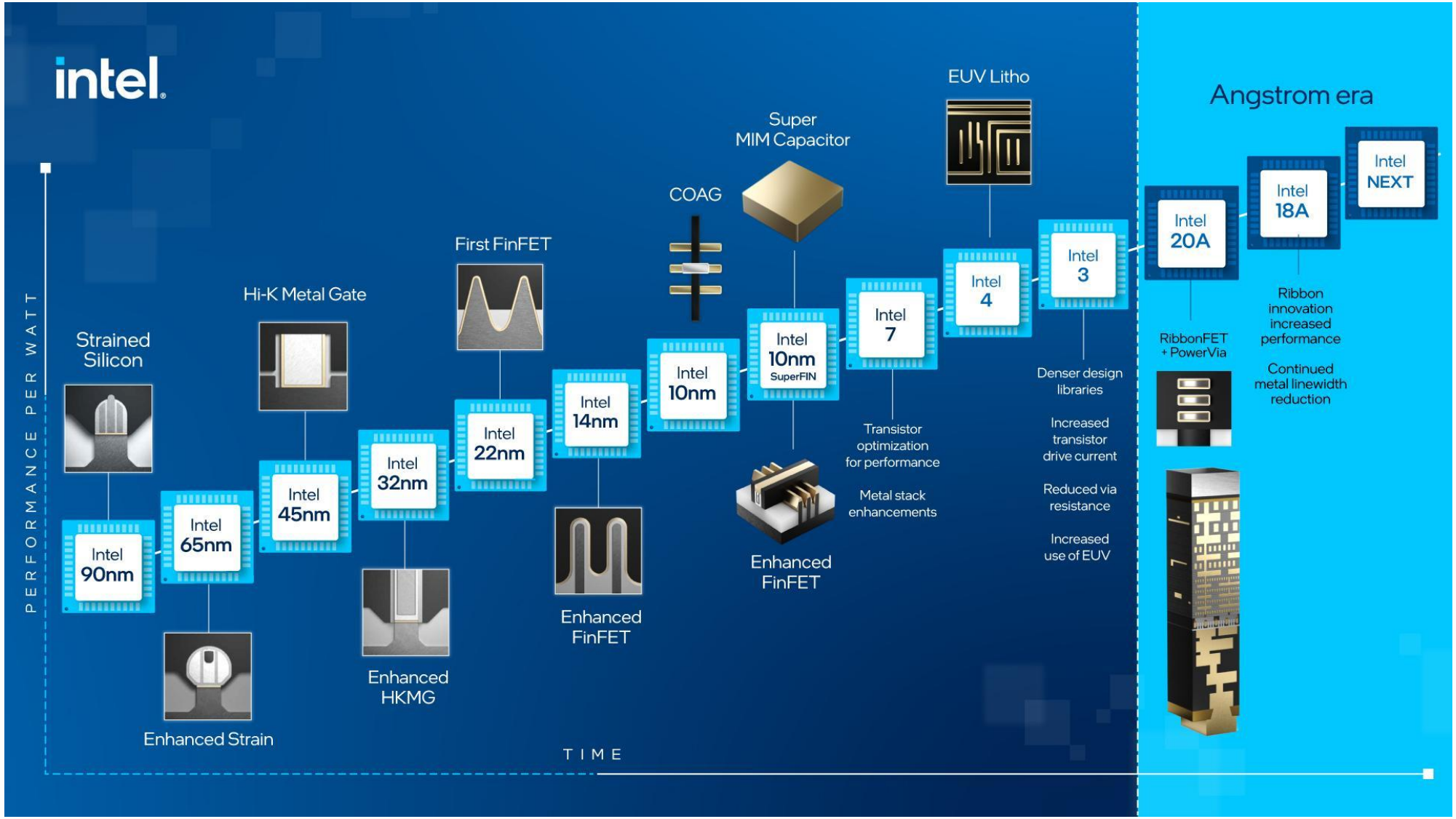
- What is VLSI?
  - Very Large-Scale Integration
  - Integration of gates or transistors?
- SSI – Small Scale Integration (0-10^2)
- MSI – Medium Scale Integration (10^2-10^3)
- LSI – Large Scale Integration (10^3-10^5)
- VLSI – Very Large-Scale Integration (>=10^7)

Analog Chip Design

- Moore's Law



Analog Chip Design



Analog Chip Design

- How to integrate millions and billions transistor?
- Solution-

  EDA Tools / CAD Tools

  Electronic Design Automation Tools
- Cadence
- Synopsys
- Mentor Graphics (Siemens)

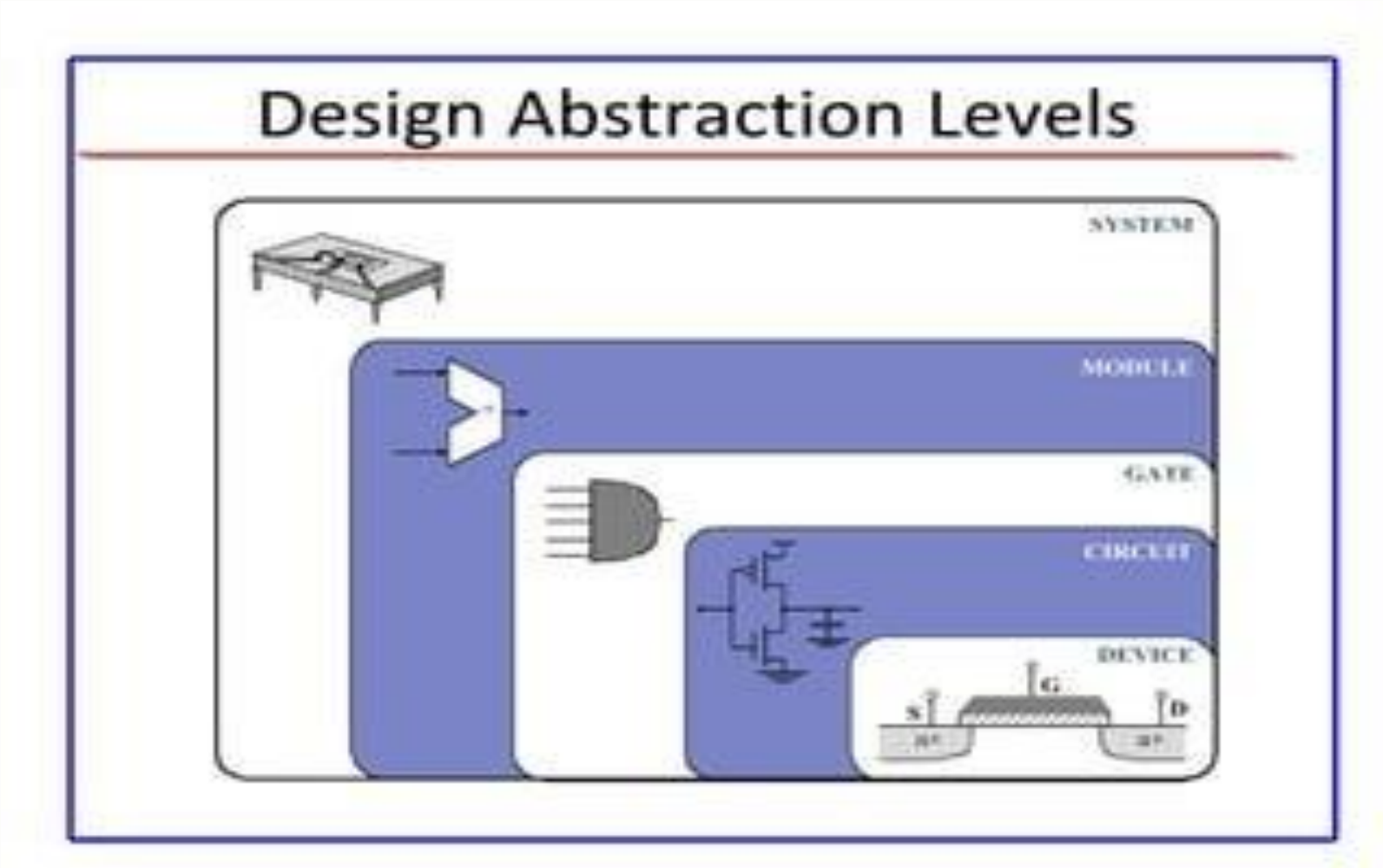
Analog Chip Design

- Front end and Back end

- Front end: initial conceptualization, system level description, architecture level, RTL coding

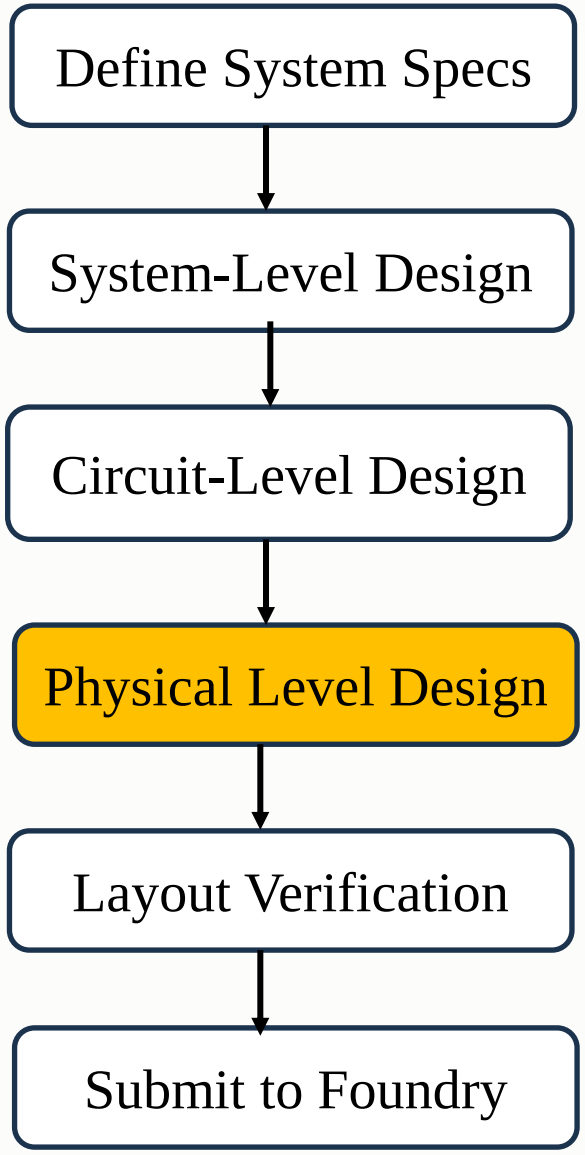
- Back end: Physical implementation, floor planning placement and routing

Analog Chip Design



Chip Design Flow Using Cadence

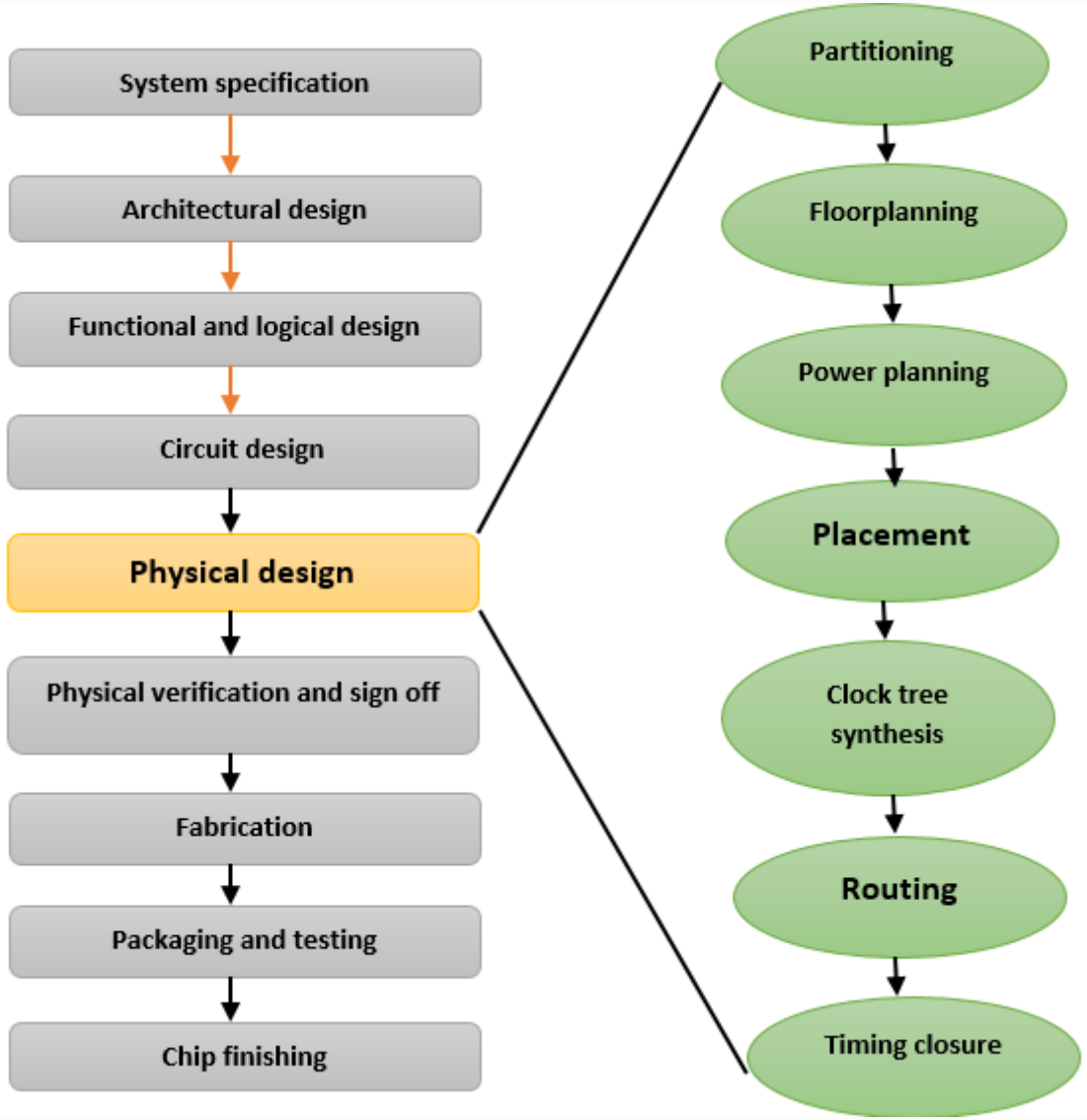
- Chip Design Flow



Schematic editor & Ckt Simulator - Spice	Device Models (Model file)
Layout editor, Design rule check (DRC)	Technology file, extraction file
Layout Vs Schematic (LVS), Spice for post layout simulation	Technology file, Device Models

Chip Design Flow Using Cadence

Chip Design Flow



Chip Design Flow Using Cadence

- Model File:

- Technology File:The technology file provides information on various aspects, including layer definitions, design rules, spacing requirements, wire widths, and other parameters that guide the layout of the integrated circuit.

- PDK (Process Design Kit) : It's a set of libraries and associated data (model files, physical verification rule files, control files for various tools) to allow you to design in a particular technology.

Chip Design Flow Using Cadence

- PDK's : Vendors – gpdk- Generic PDK

SCL (Semi-conductor Laboratory)

UMC – (United Microelectronics Corporation)

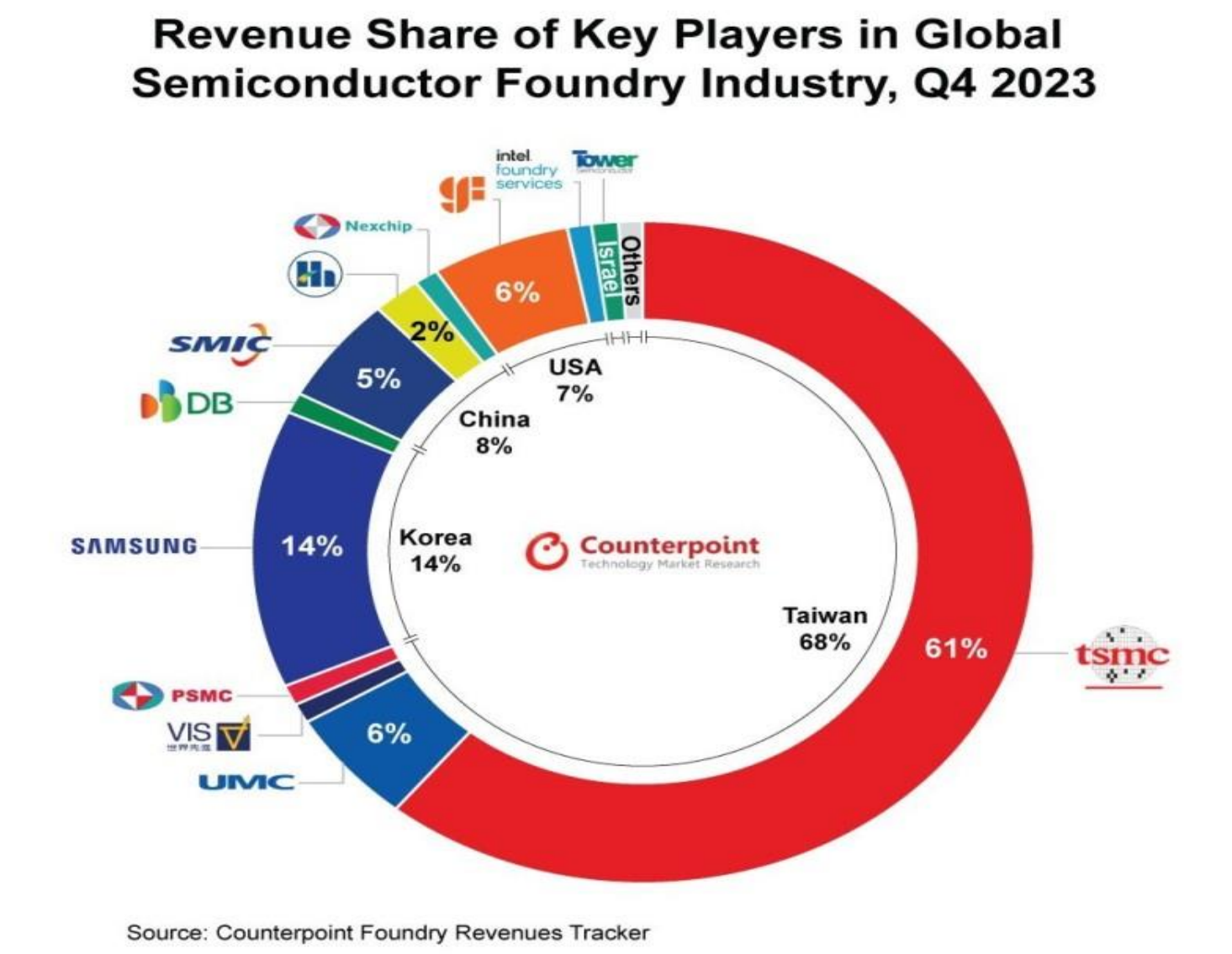
TSMC – (Taiwan Semiconductor Manufacturing Company)

Tower Semiconductor

Global Foundries

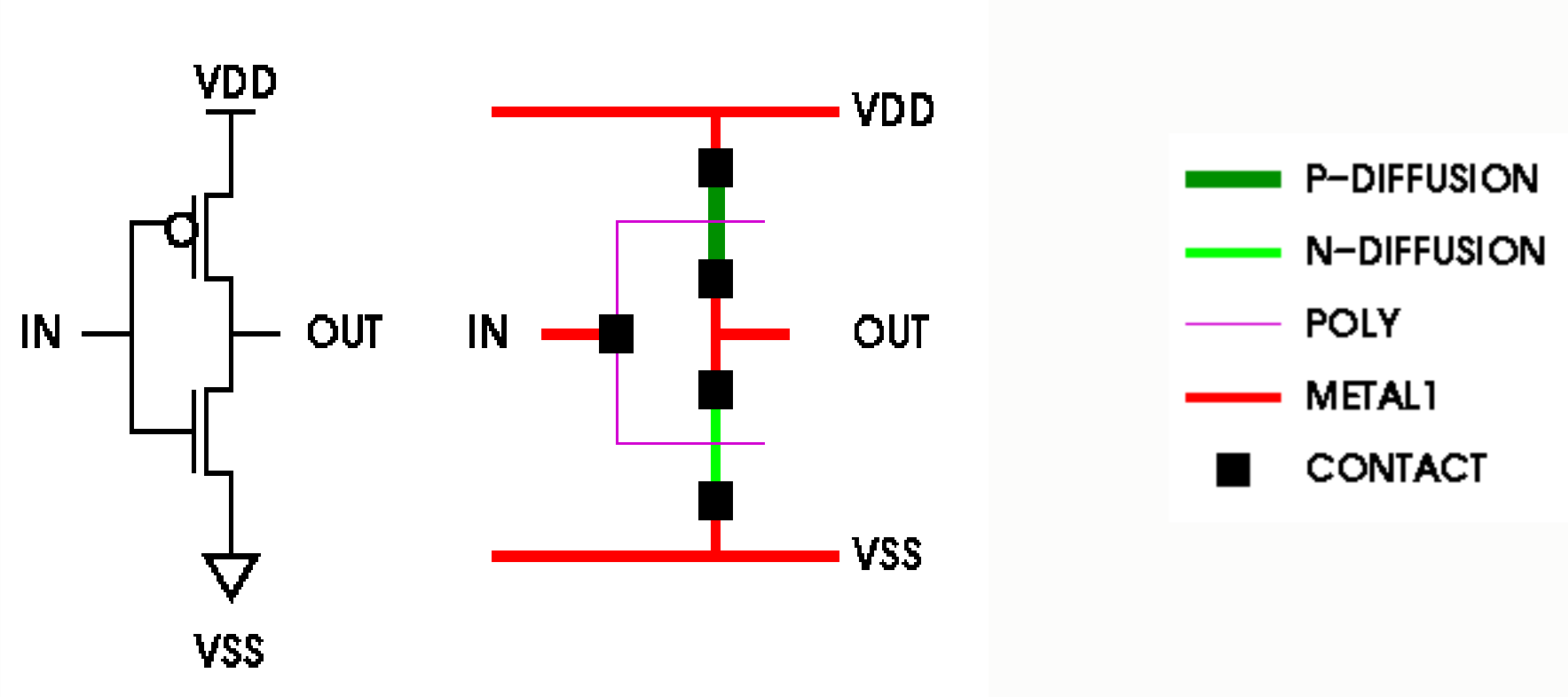
SMIC – (Semiconductor Manufacturing International Corporation)

Chip Design Flow Using Cadence



Chip Design Flow Using Cadence

✓ CMOS Inverter and Stick Diagram



Chip Design Flow Using Cadence

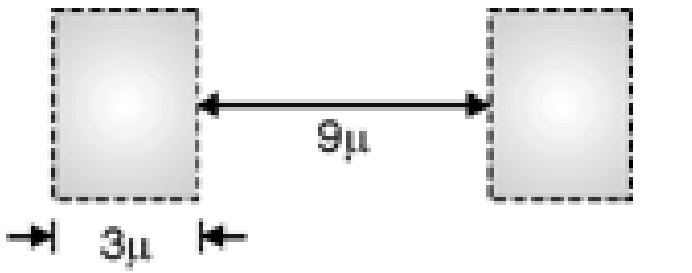
- Layout Design Rules
  - Lambed Based Design Rules
  - Micron based Design Rules

- Lambed Based Design Rules
  - Expressed in terms of a scaling parameter: Lambda (λ)
  - Minimum line width: 2 λ
  - Main disadvantages:
    - Limited linear scaling
    - Too conservative

Chip Design Flow Using Cadence

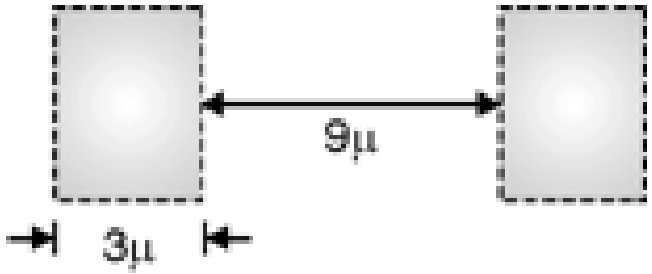
- Micron Based Design Rules
  - Express designs in absolute dimensions
  - Pro: Allow taking full advantage of technology
  - Con: Scaling and Porting becomes more complicated

- (1) Rules for N-well as shown in Figure below.
  - Width 3μ
  - Space 9μ



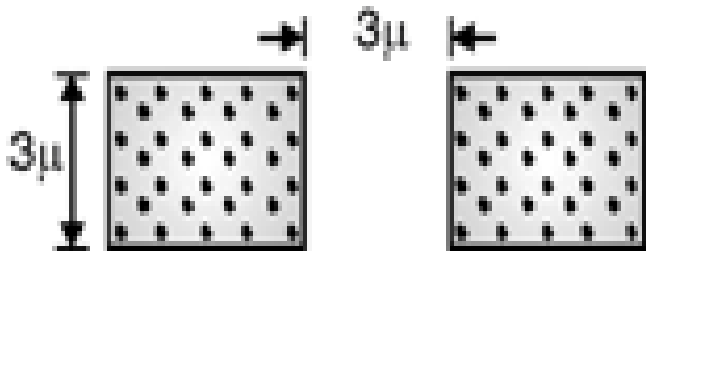
Chip Design Flow Using Cadence

- 2) Rules for active area as shown in Figure below
  - 1. Minimum size = 3μ
  - 2. Minimum spacing = 3μ
  - 2. N+ active to N-well = 7μ



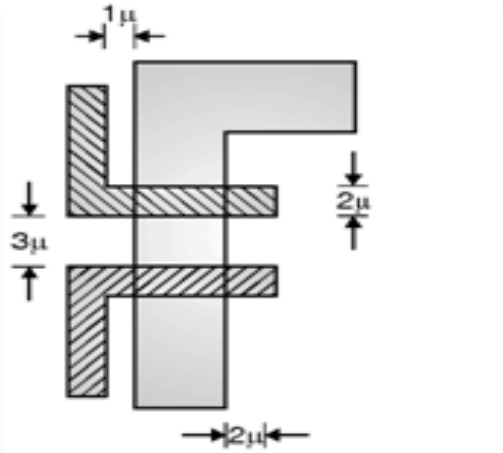
(3) Rules for poly 1 as shown in Figure below.

1. Width = 2μ
2. Spacing = 3μ
3. Gate overlap of active = 2μ
4. Field poly 1 to active = 1μ

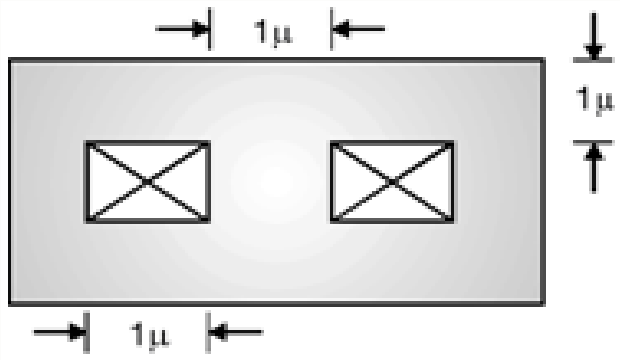


Chip Design Flow Using Cadence

- 4) Rules for contact to Poly as shown in Figure below
  - 1. Exact contact size = 2μ x 2μ
  - 2. Minimum Poly overlap = 1μ
  - 3. Minimum contact spacing = 2μ

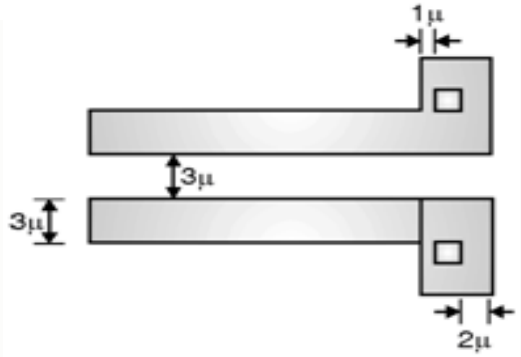


- (5) Rules for contact to Active as shown in Figure below.
  1. Exact contact size = 2μ x 2μ
  2. Minimum active overlap = 1μ
  3. Minimum contact spacing= 2μ
  4. Minimum spacing to gate= 2μ

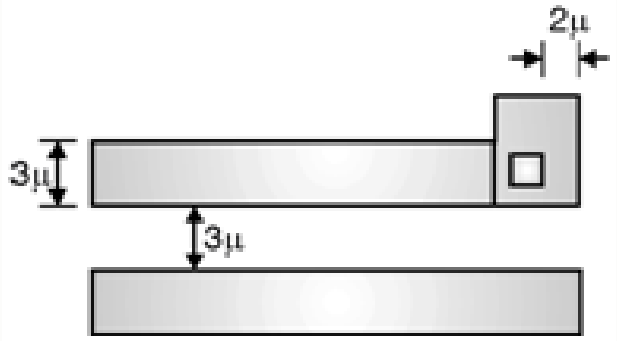


Chip Design Flow Using Cadence

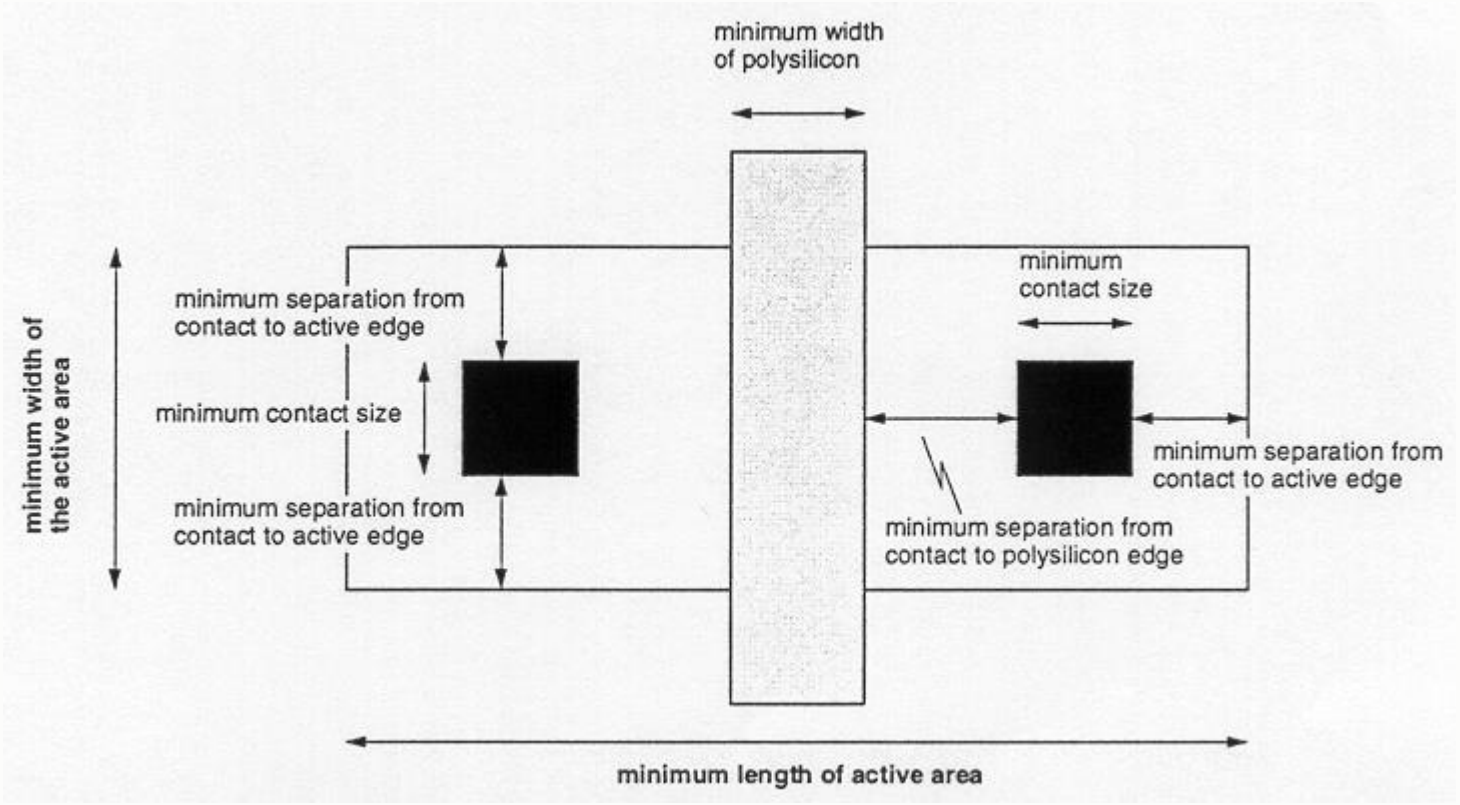
- 6) Rules for Metal 1 as shown in Figure below
  - 1. Width = 3μ
  - 2. Spacing = 3μ
  - 3. Overlap of contact = 1μ



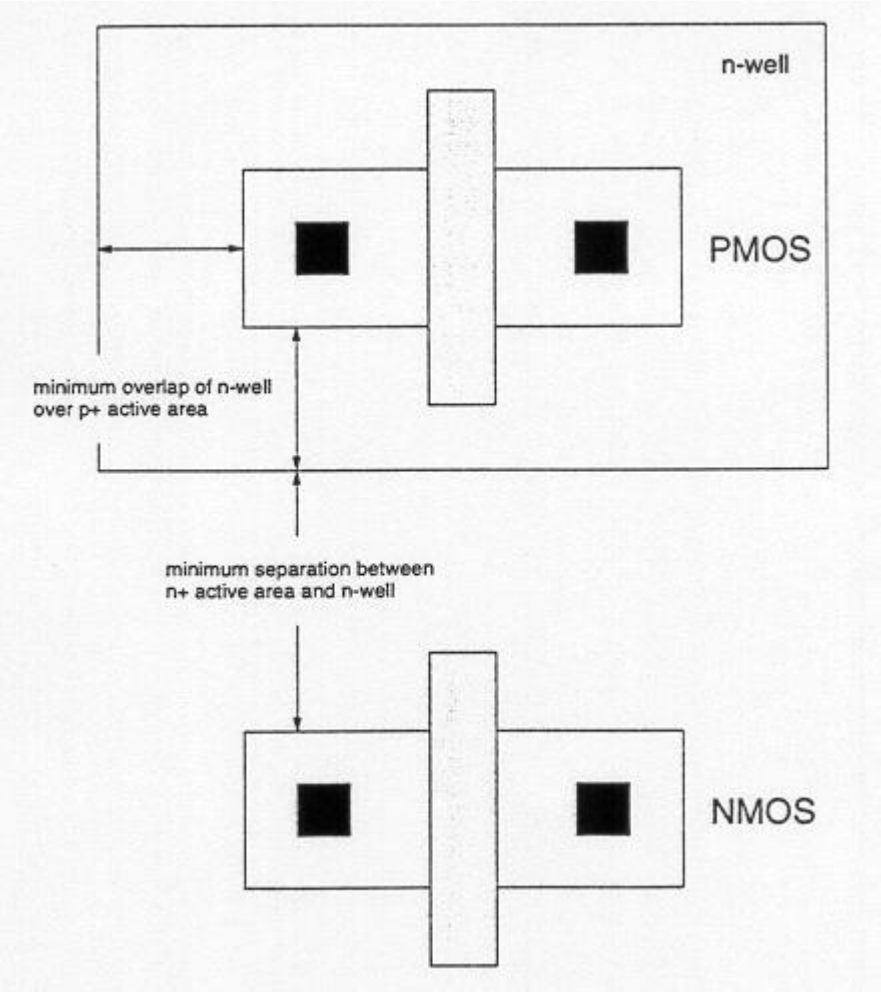
- (7) Rules for Metal 2 as shown in Figure below.
  1. Width = 3μ
  2. Spacing = 3μ
  3. Overlap of contact = 1μ



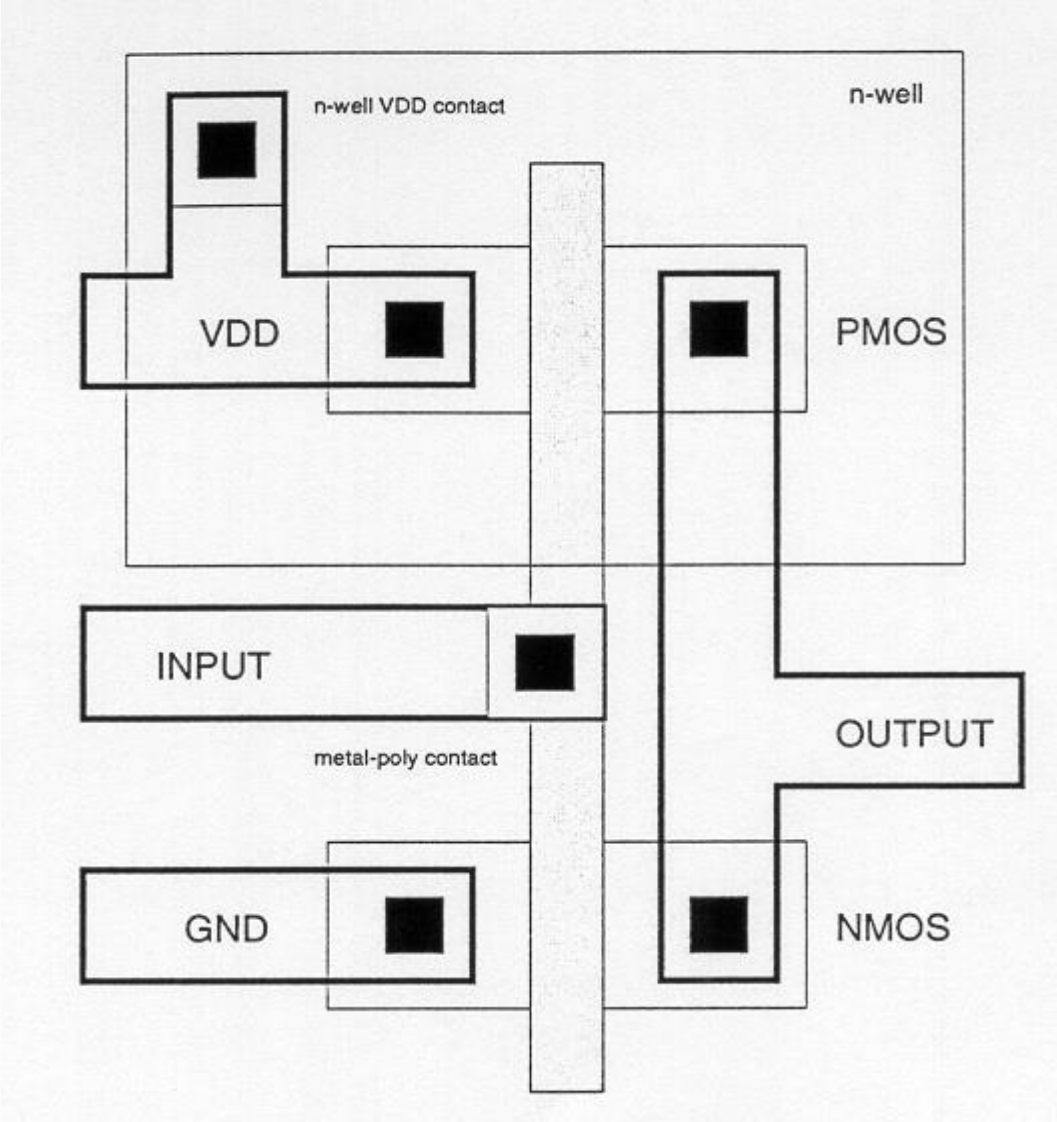
Chip Design Flow Using Cadence



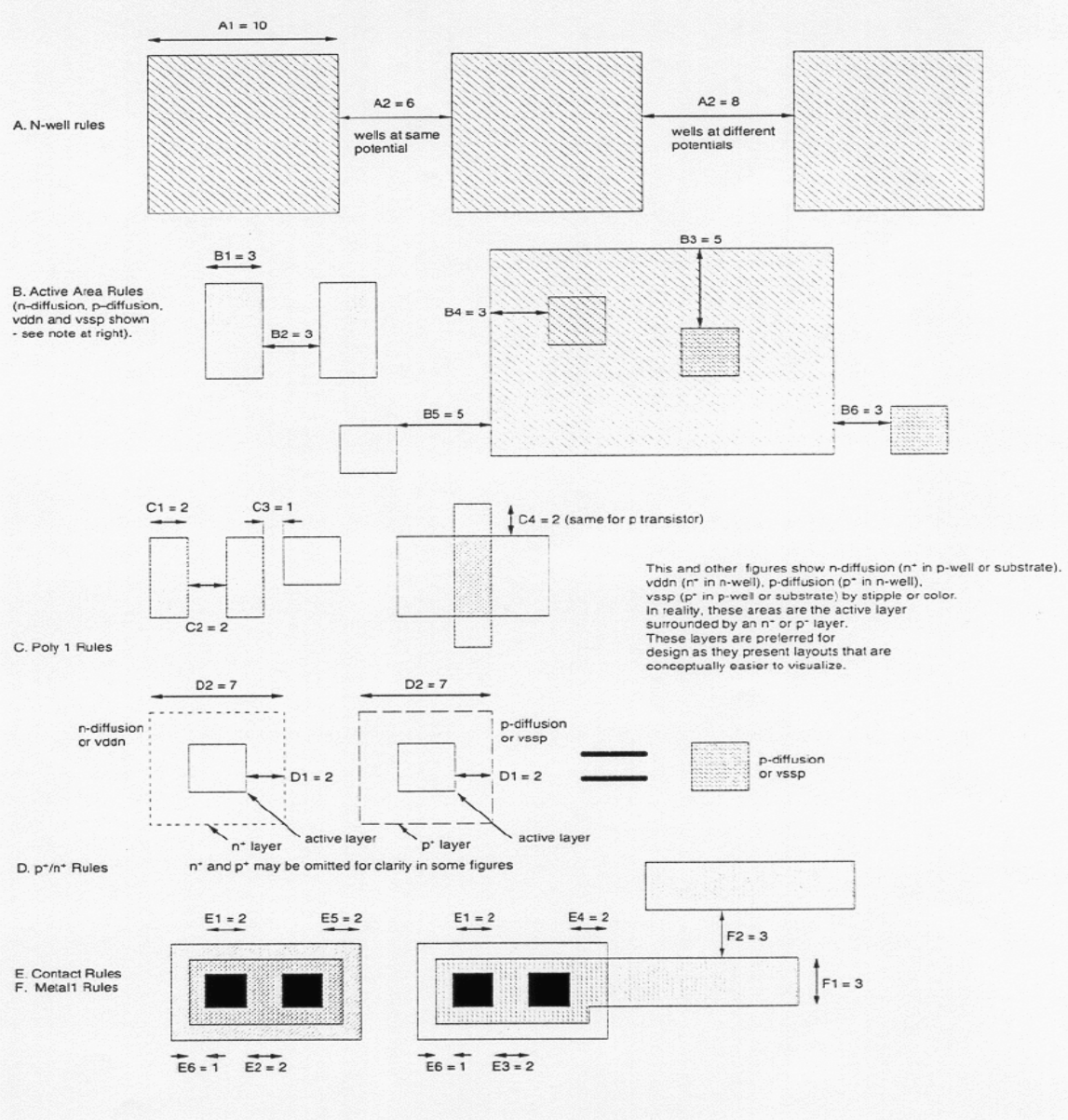
Chip Design Flow Using Cadence



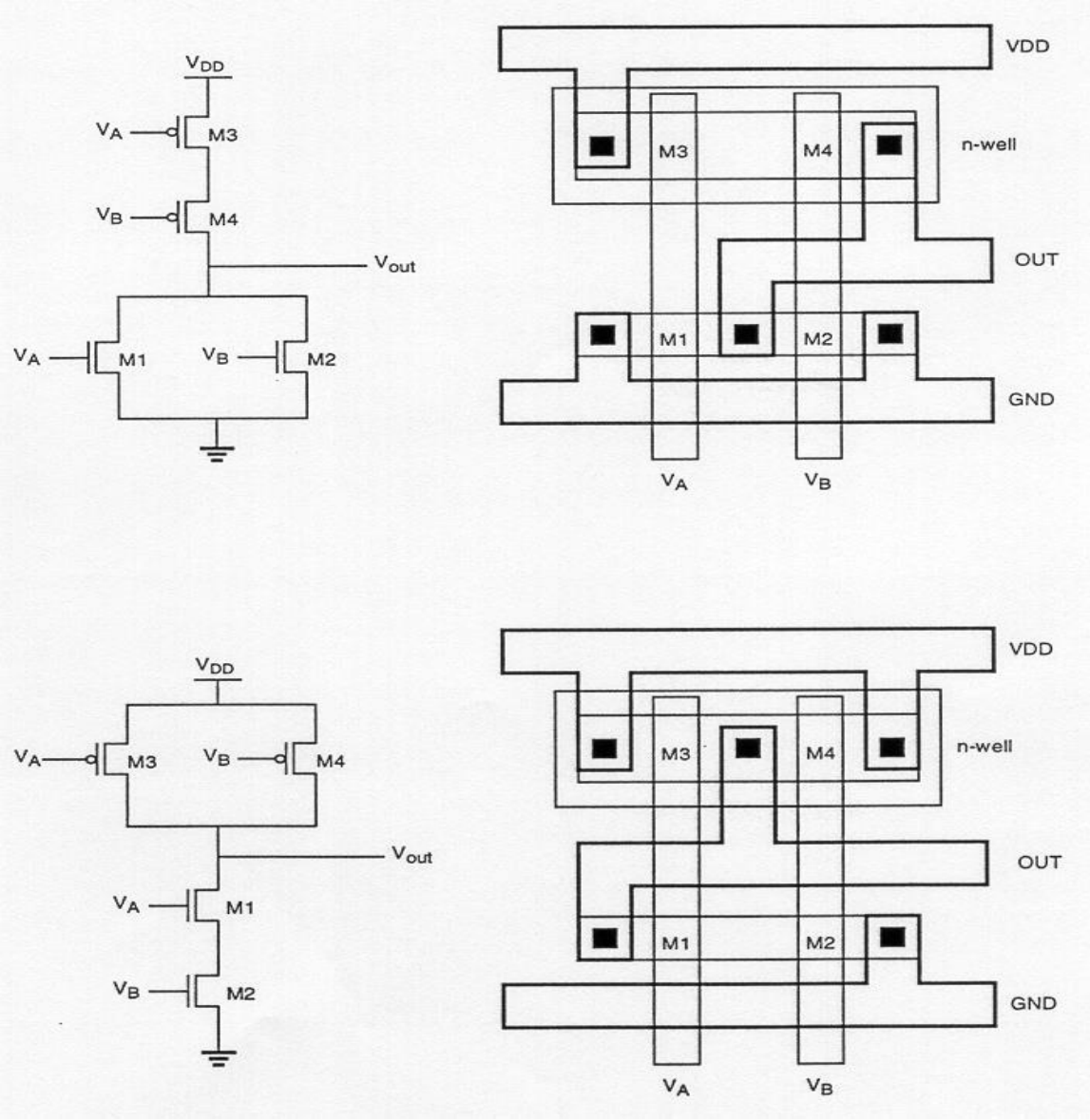
Chip Design Flow Using Cadence



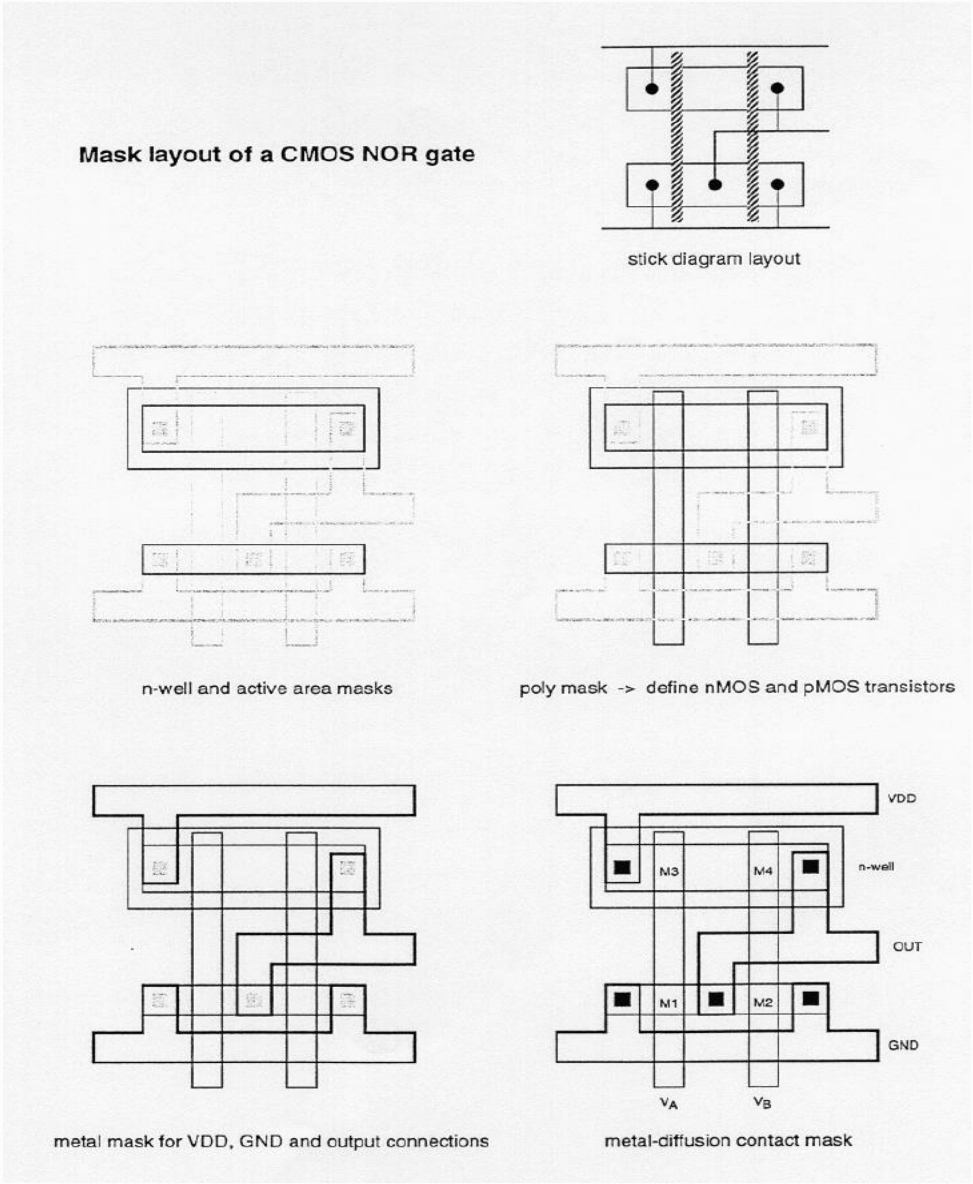
Chip Design Flow Using Cadence



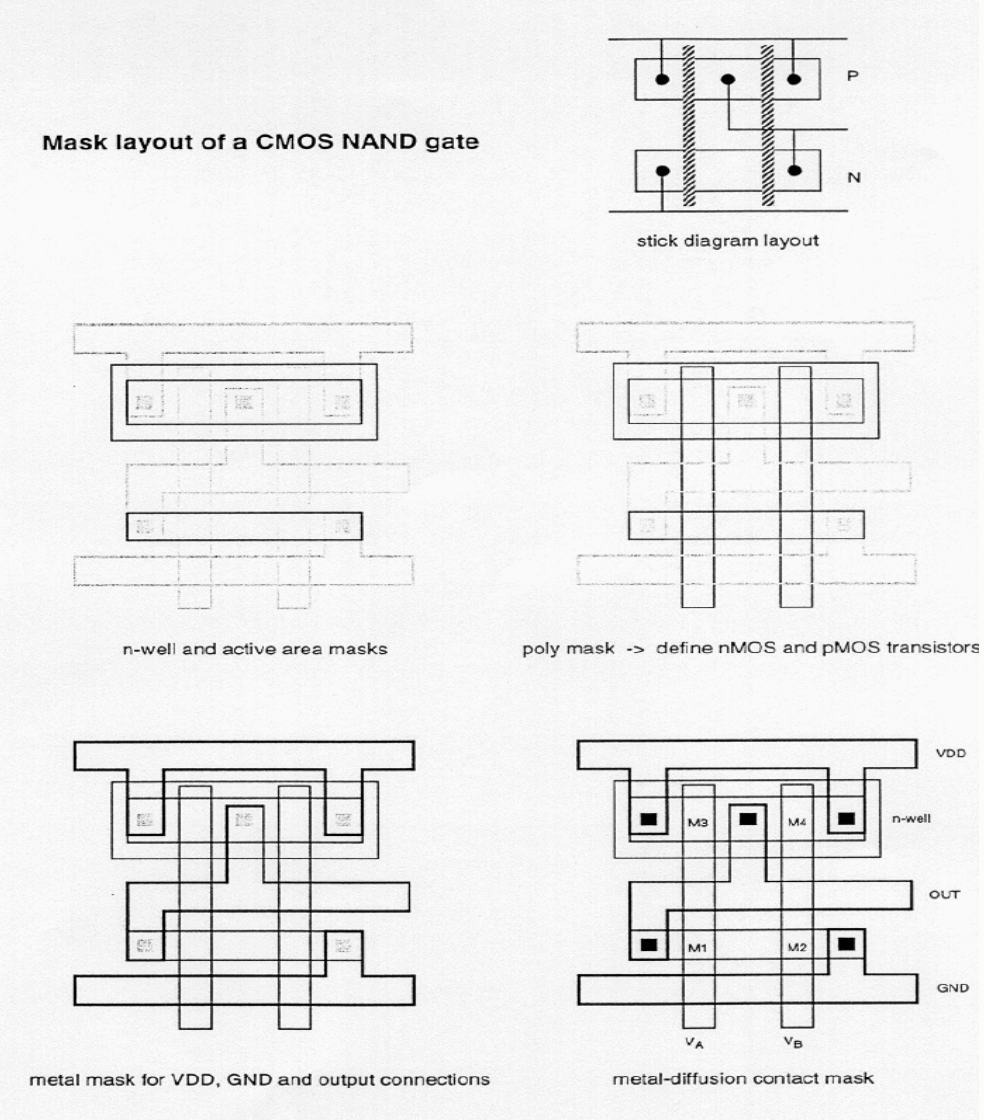
Chip Design Flow Using Cadence



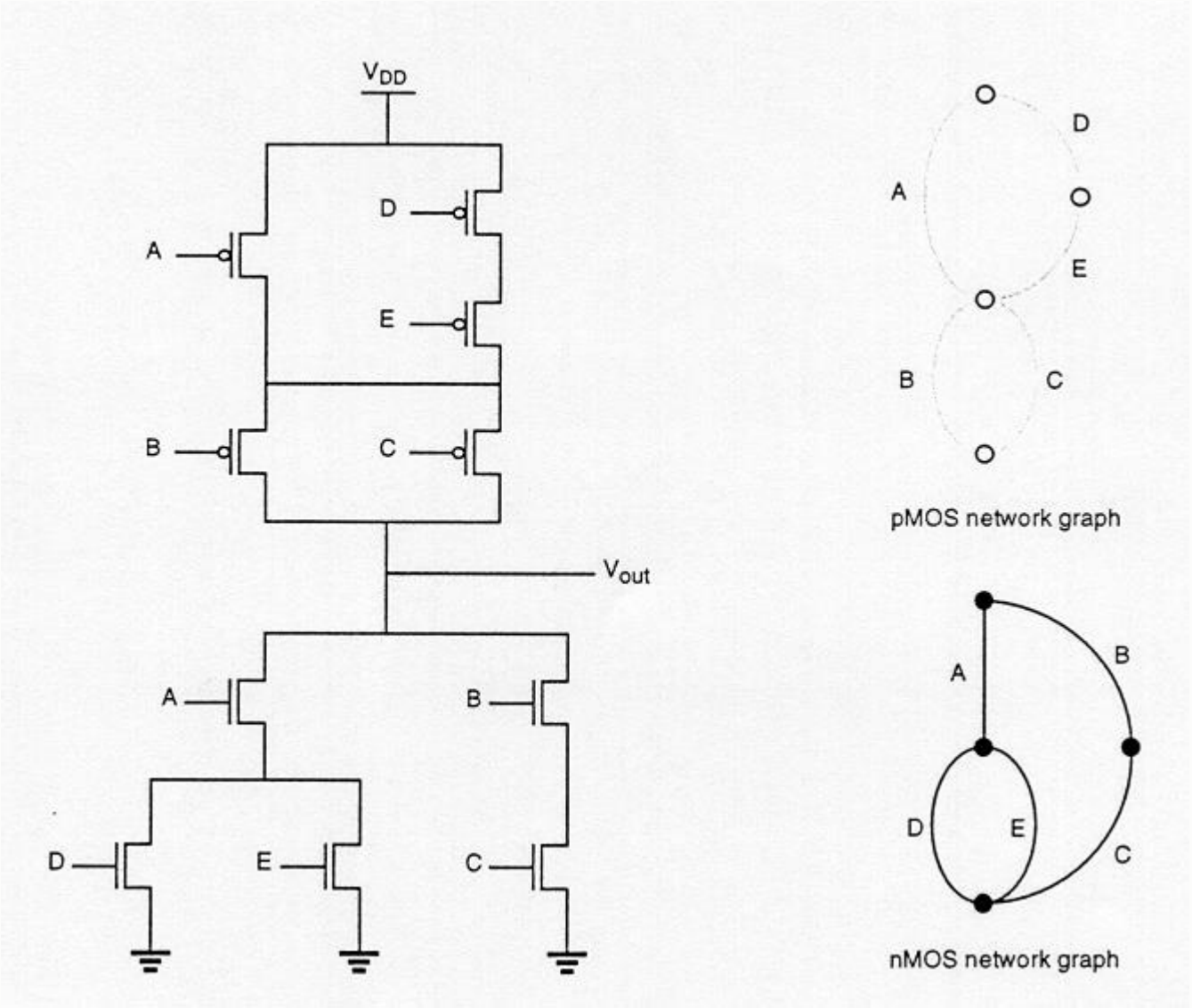
Chip Design Flow Using Cadence



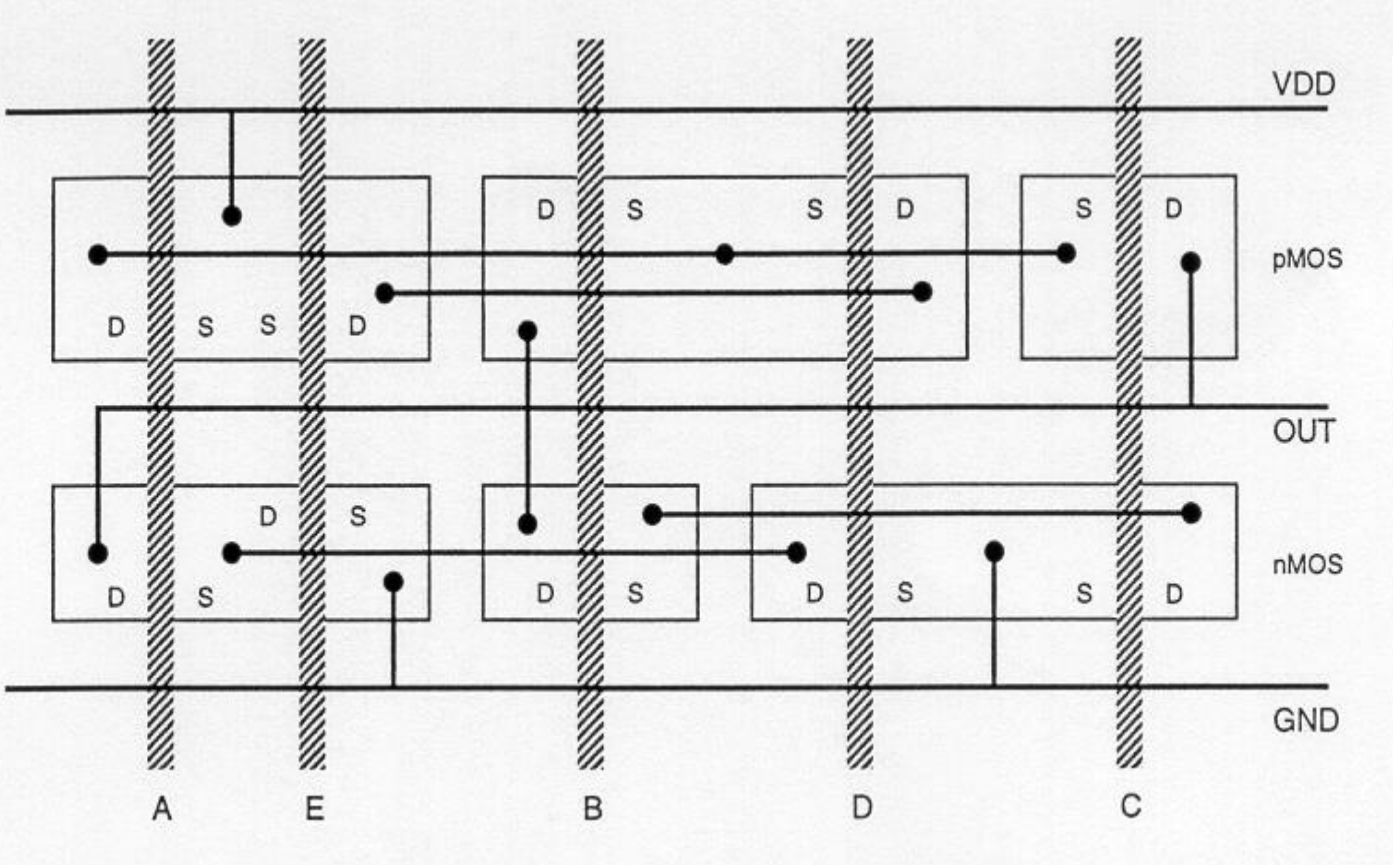
Chip Design Flow Using Cadence

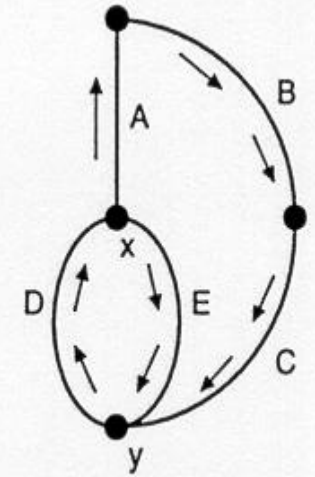


Chip Design Flow Using Cadence



Chip Design Flow Using Cadence

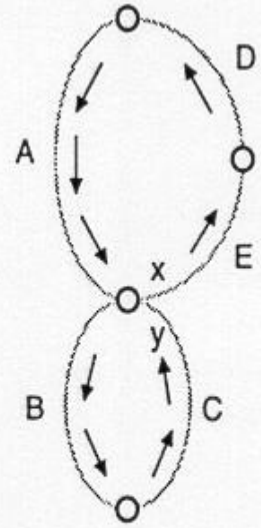




nMOS network graph

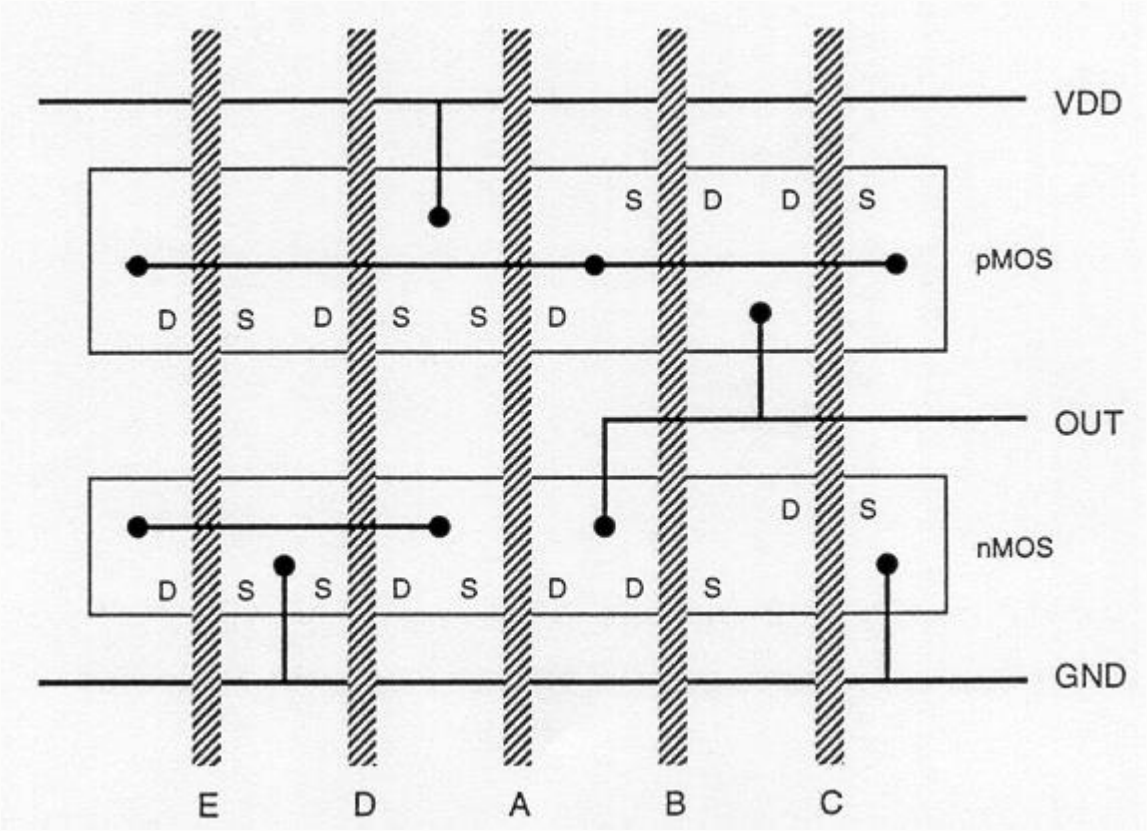
Common Euler path :

E - D - A - B - C



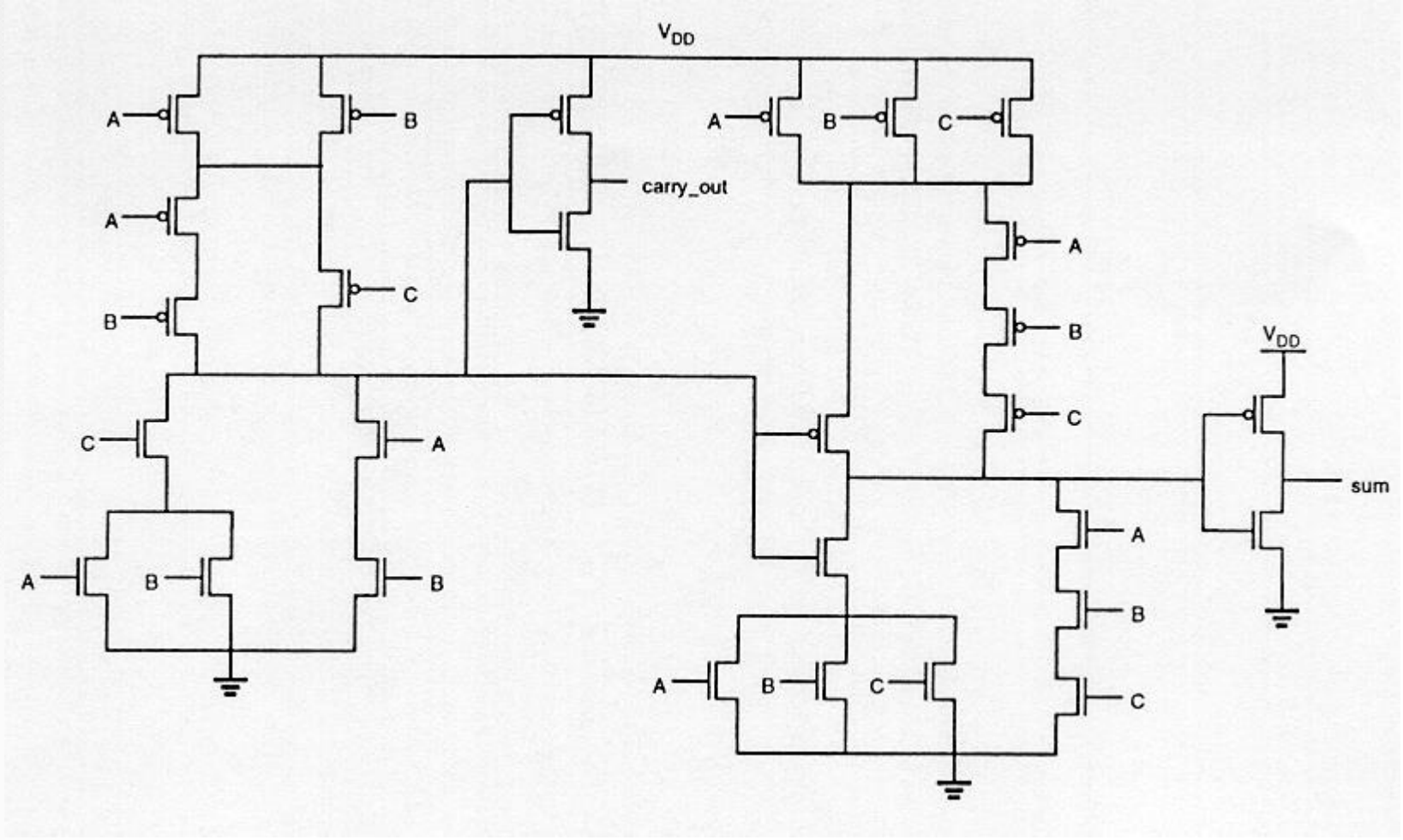
pMOS network graph

Chip Design Flow Using Cadence



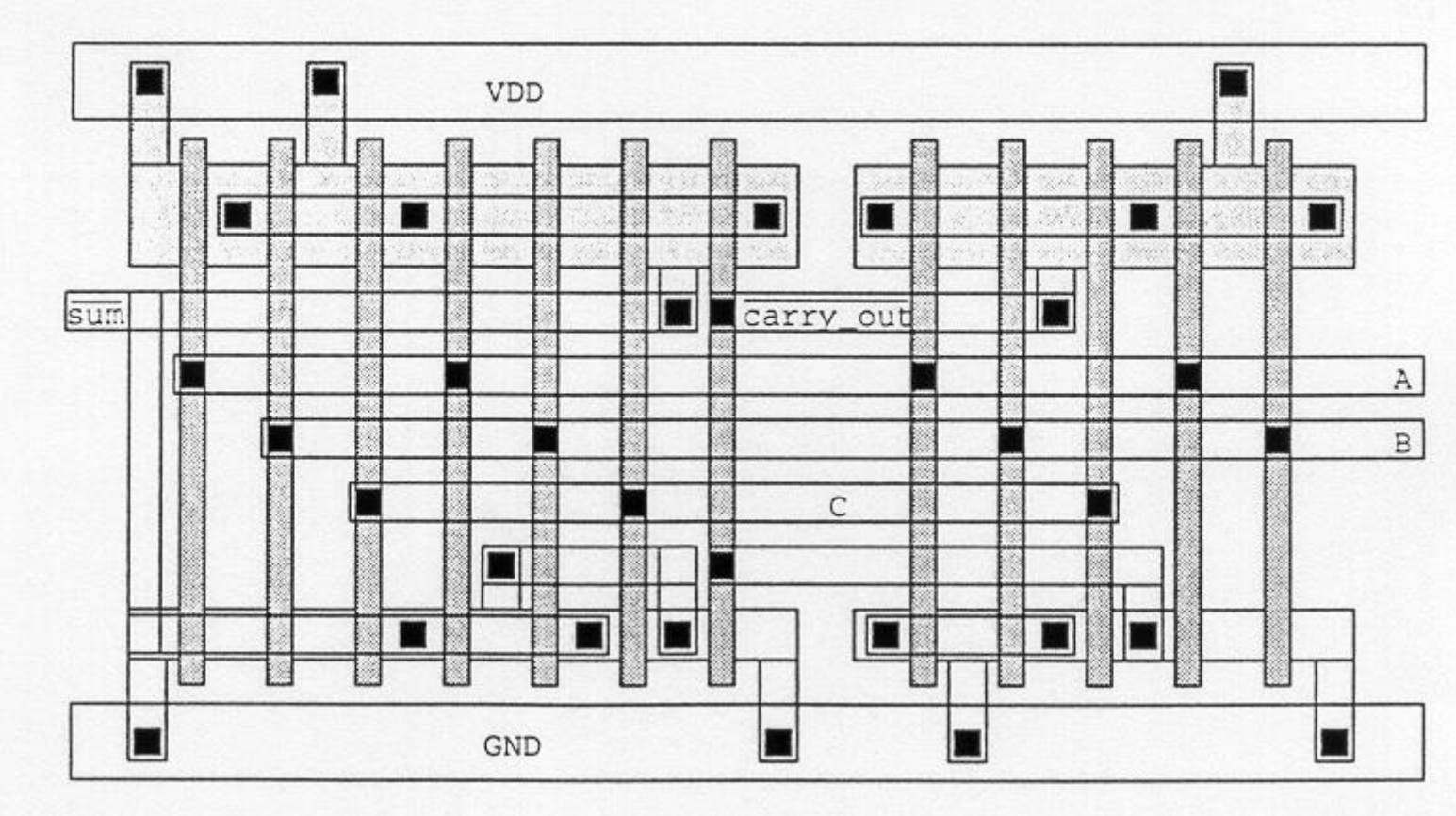
Chip Design Flow Using Cadence

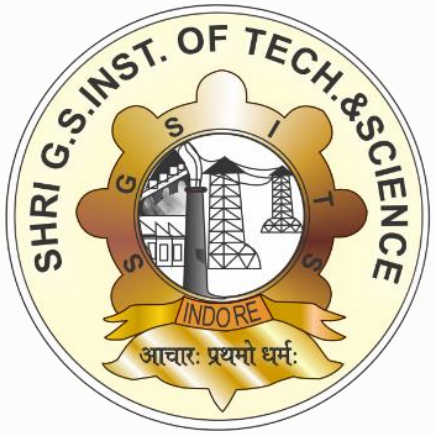
✓ **Full Adder**



Chip Design Flow Using Cadence

✓ **Full Adder Layout**





THANK YOU