MODULE 3

VLSI DESIGN

17EC63/15EC63

STICK DIAGRAMS

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Introduction

- A popular method of symbolic design ---- stick layout.
- Designer draw a free hand sketch of a Layout, using coloured lines to represent various process layers such as ***Diffusion (p or n) , Metal and Poly-silicon where***

Polysilicon layer crosses diffusion ------- Transistor are created.

Metal wires join Diffusion or poly ------- contacts are formed.

- Design rules are communication link b/w the designer specifying requirements and fabricator who materializes them. VLSI design aims to translate circuit concepts onto silicon.
- First set of Design rules were introduced by Lambda based.

- Mask design is aimed at turning a specification into masks for processing silicon to meet the specification.
- Stick Diagrams may be used to convey the layer information through the use of colour code.
- **Note**: For Depletion mode transistor, Implant within the thin oxide is a must.
- Stick diagram and mask layout is one and the same ,but in mask layout ,aspect ratio (L:W) & distance between any dimensions has to be shown.
- ***Nwell CMOS inverter***:

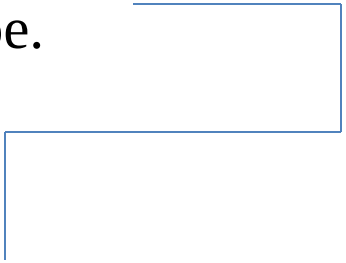
  In CMOS ,we have both pmos and nmos on same substrate, so we take P-substrate and create n-well.

  Apply V_{DD} to all well in mask layout.

- N-well CMOS circuit are superior to p-well because of lower substrate bias effects on transistor threshold and inherently low parasitic capacitances associated with source and drain regions.
- For students ,some of the hints are:

if transistors are in parallel ----- construct active layer in U shape .

if transistors are in series combination ----- construct active layer in zigzag shape.



Demarcation Line (Brown) - - - - -

In mask layout , n-well has to be created.

P-type transistors are placed above and n-type are place below the demarcation line.

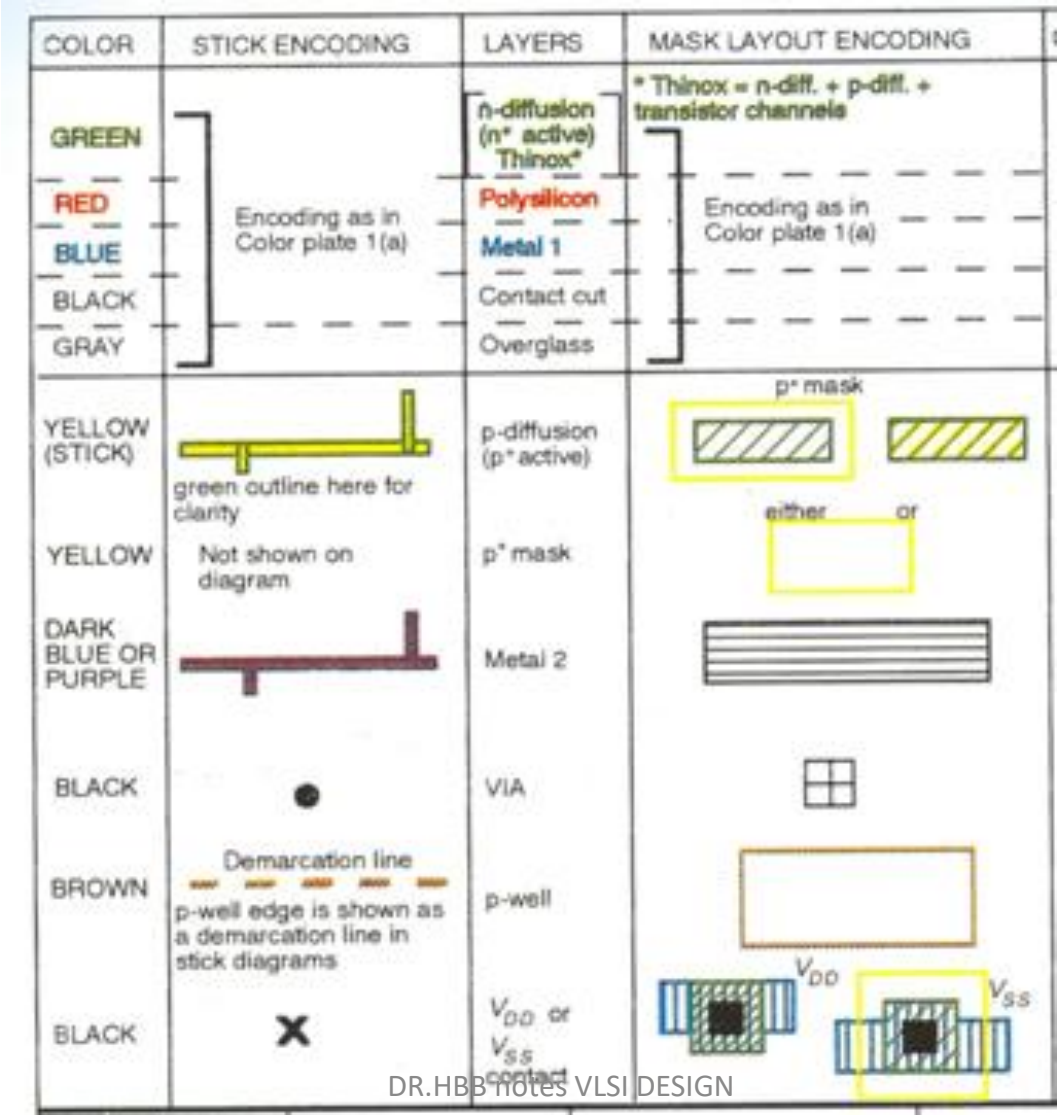
- In cmos ,no depletion tr is used.
- In cmos ,Diffusion path must not cross demarcation line.
- n Diffusion and Diffusion wires must not join. ‘n’ and ‘p’ features are normally joined by metal where a connection is needed.
- We should not forget to place a cross on Vdd and Vss rails to represent the substrate and p well respectively.
- Metal and poly-silicon can cross demarcation line.

- Does ***not*** show
  - Exact placement of components
  - Transistor sizes
  - Wire lengths, wire widths, tub boundaries.
  - Any other low level details such as parasitics..

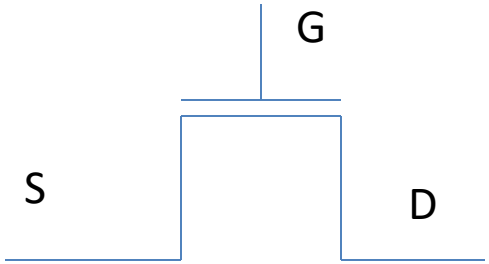
ENCODING FOR SINGLE METAL NMOS PROCESS

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING
GREEN		n-diffusion (n^+ active) Thinox*	 *Thinox = n-diff. + transistor channels
RED		Polysilicon	
BLUE		Metal 1	
BLACK		Contact cut	
GRAY	NOT APPLICABLE	Overglass	
nMOS ONLY YELLOW		Implant	
nMOS ONLY BROWN		Buried contact	

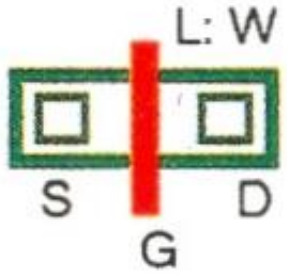
Encodings for CMOS process



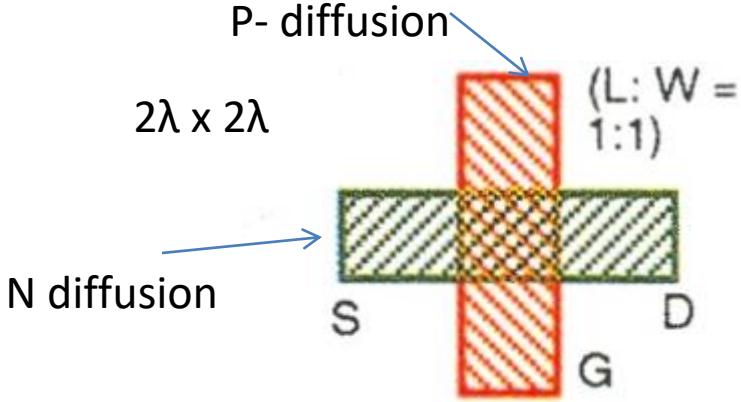
N type enhancement mode transistor



STICK DIAGRAM

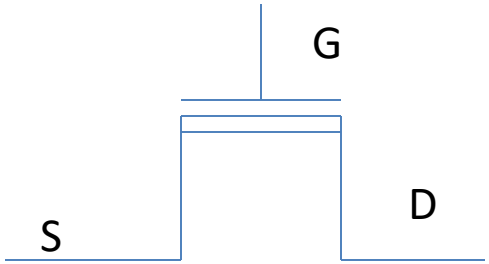


SYMBOL

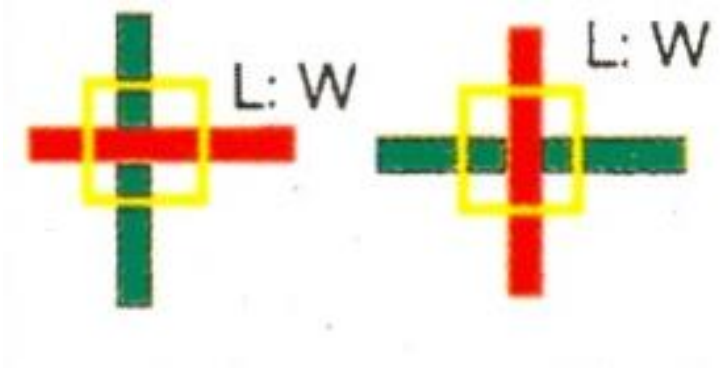


MASK LAYOUT

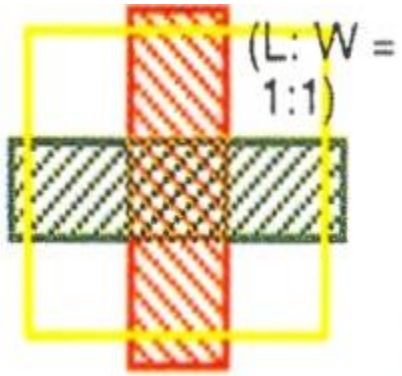
N type depletion mode transistor



STICK DIAGRAM

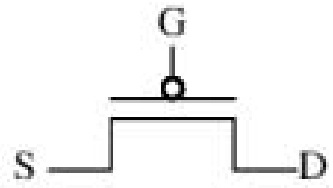


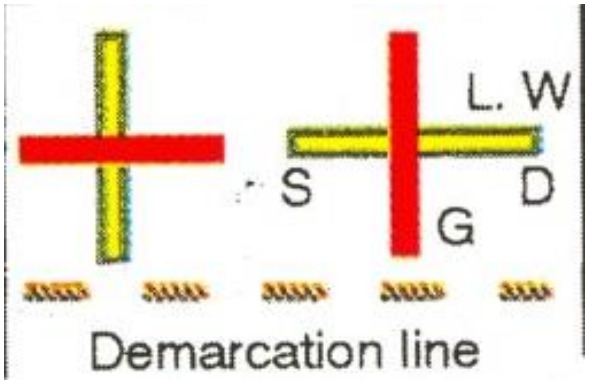
SYMBOL

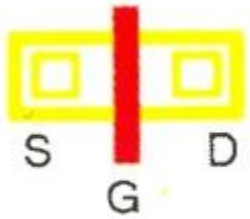


MASK LAYOUT

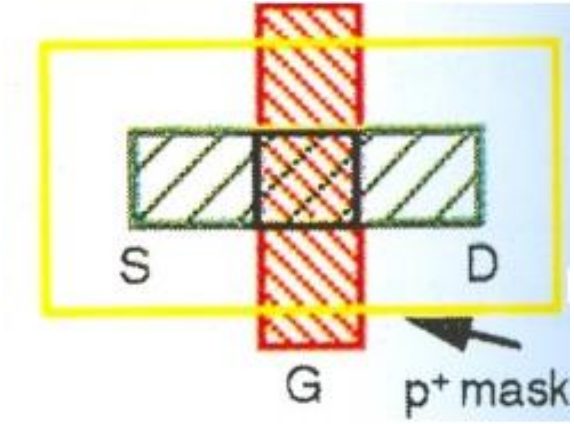
P type enhancement mode transistor in cmos p-well process



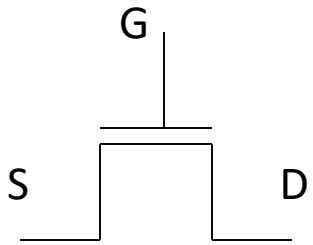


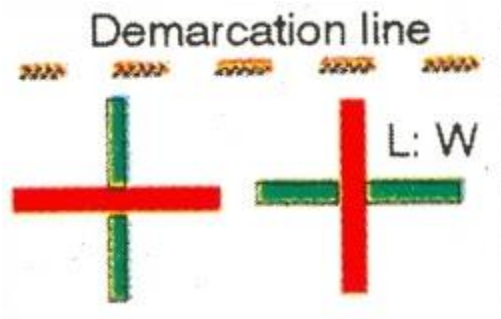


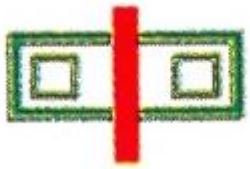
SYMBOL



N type enhancement mode transistor in cmos p-well process

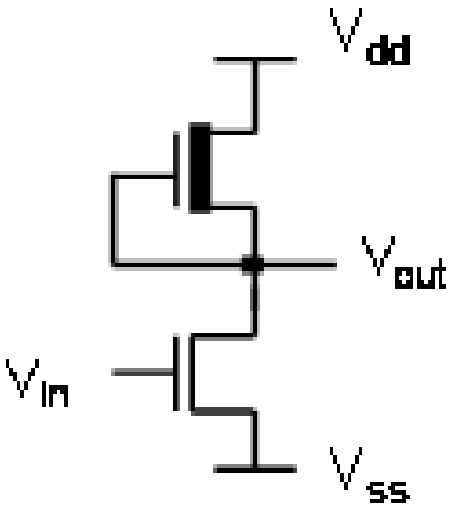




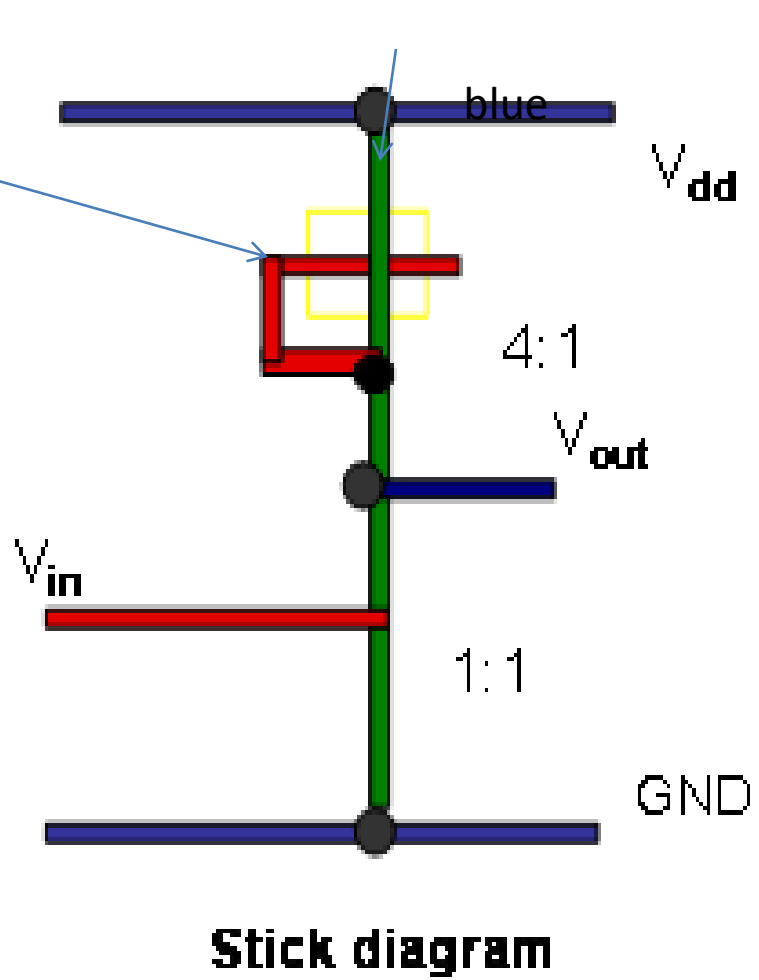


SYMBOL

nMOS depletion load inverter

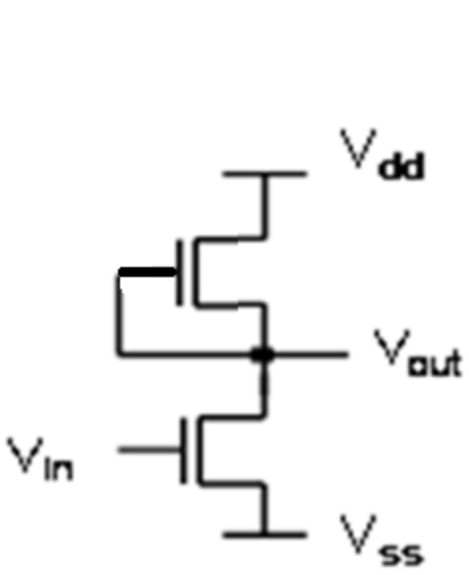


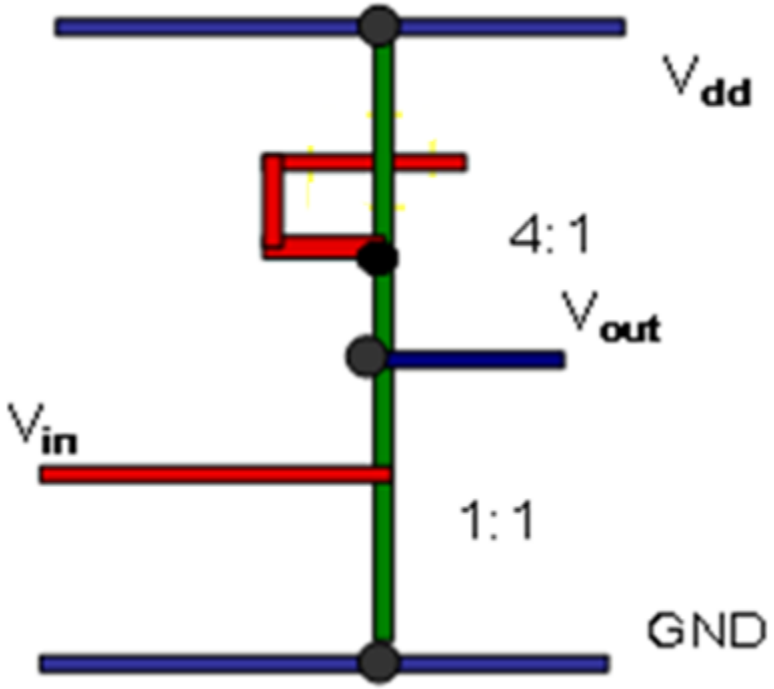
Schematic



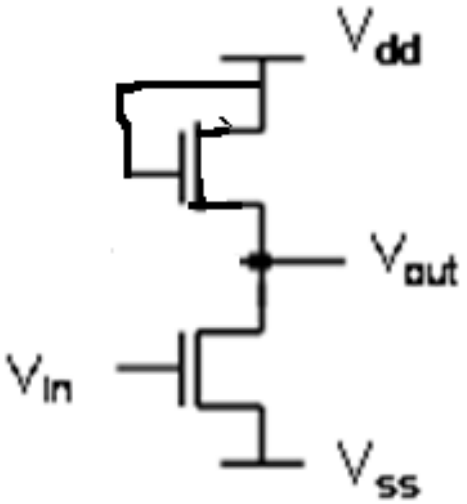
Stick diagram

nMOS enhancement load inverter





nMOS enhancement load inverter



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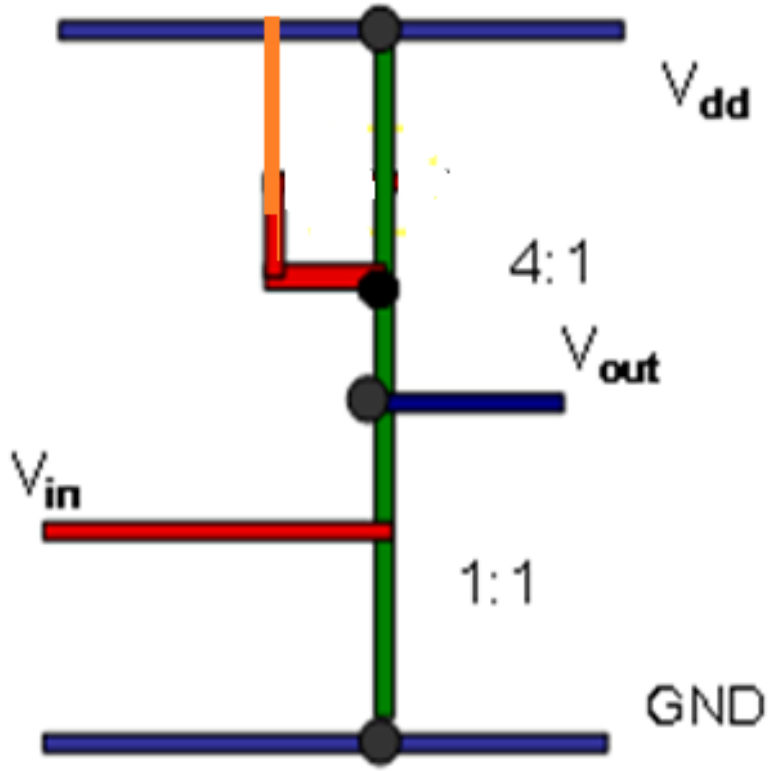
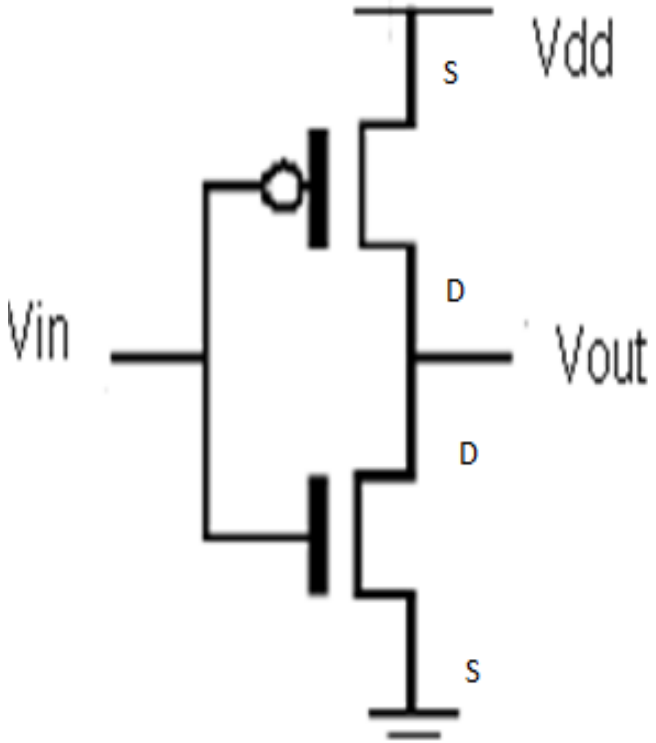
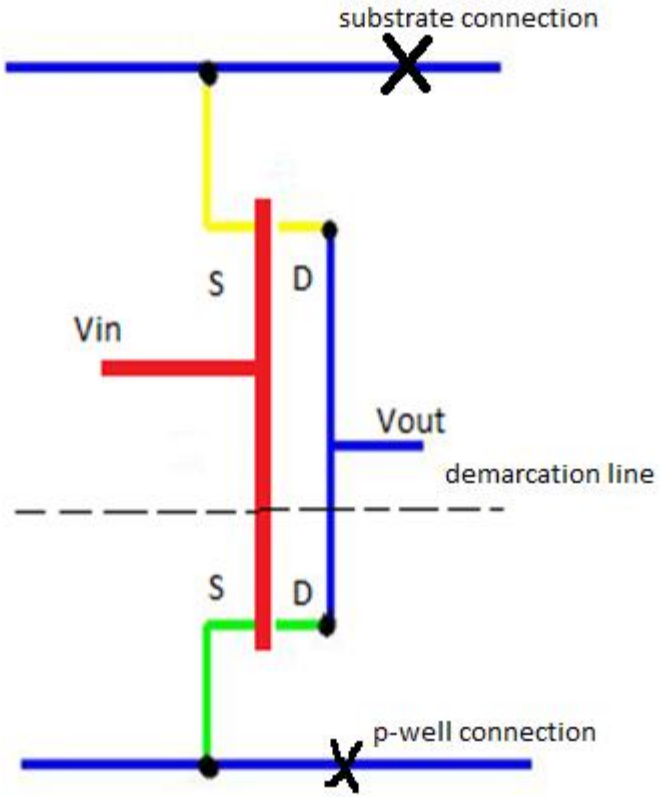


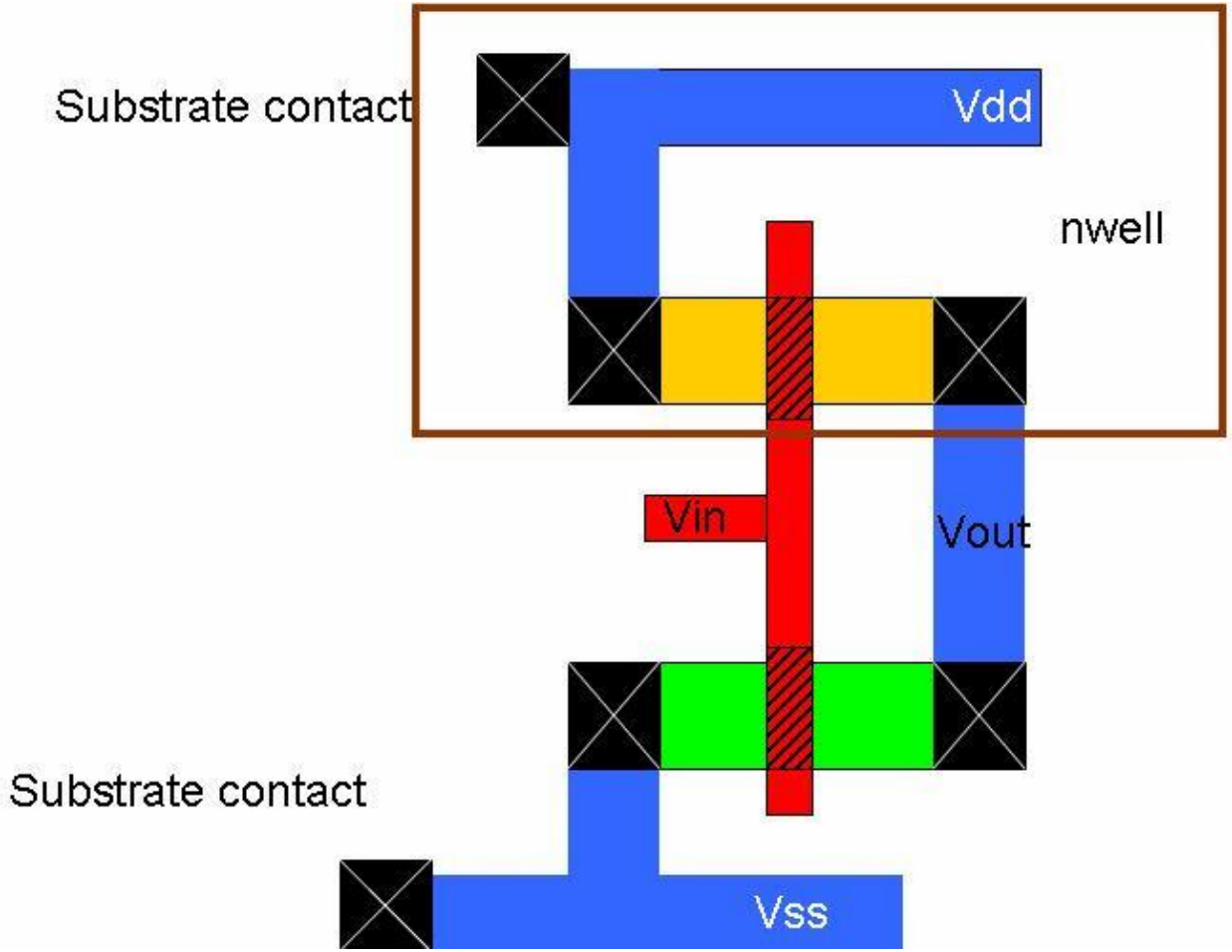
Stick diagram

CMOS INVERTER

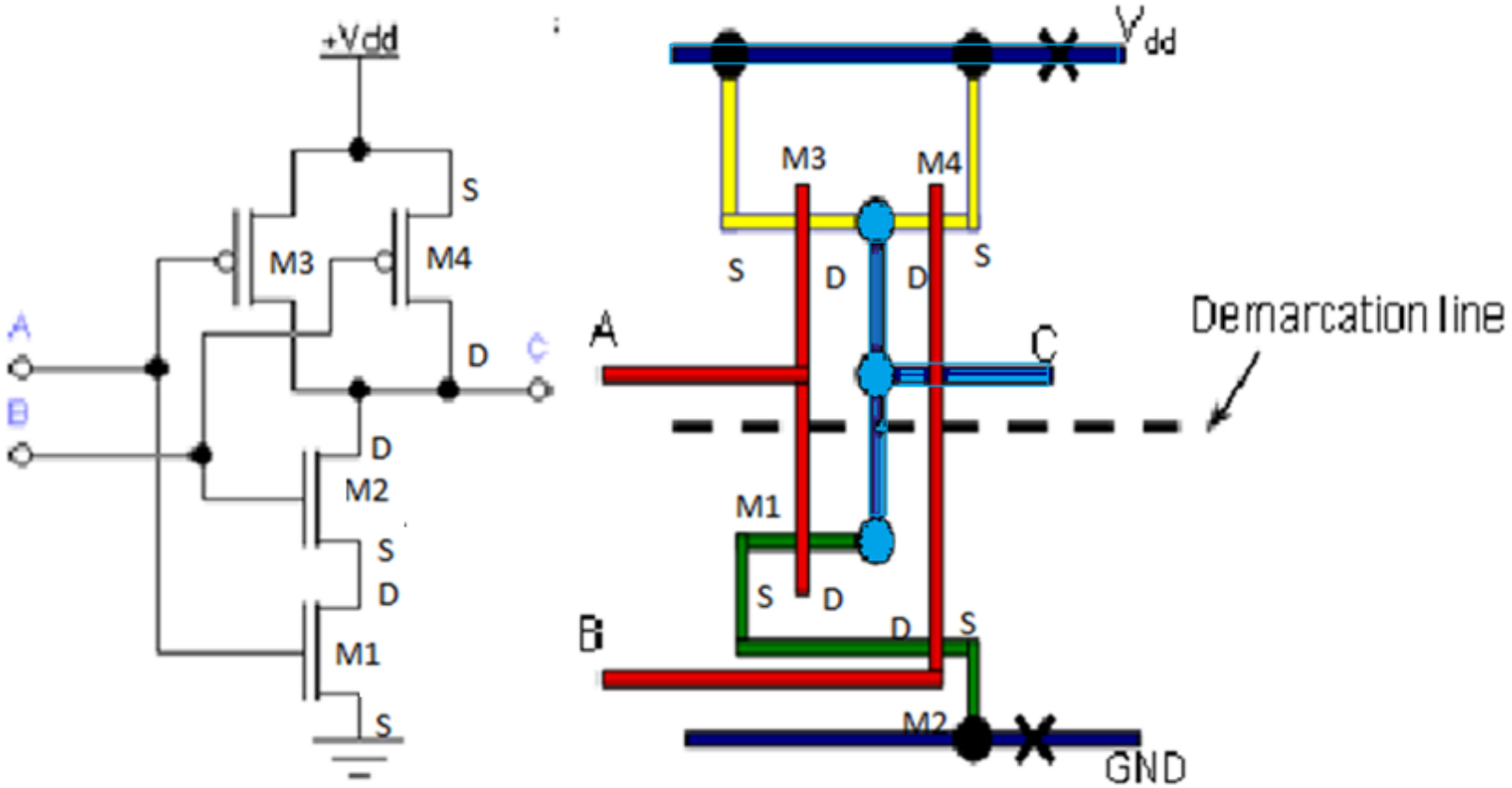




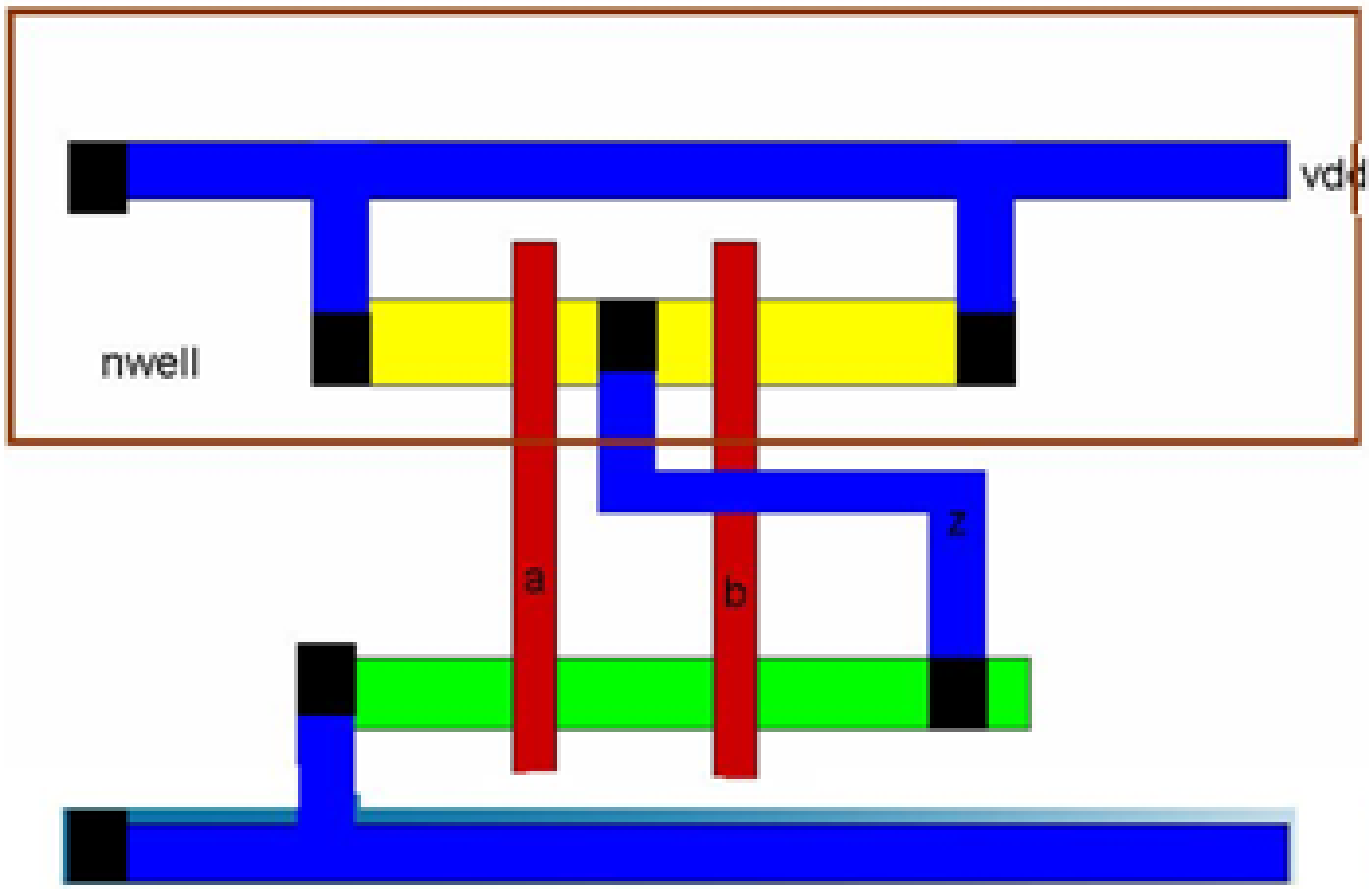
Mask layout – CMOS INVERTER



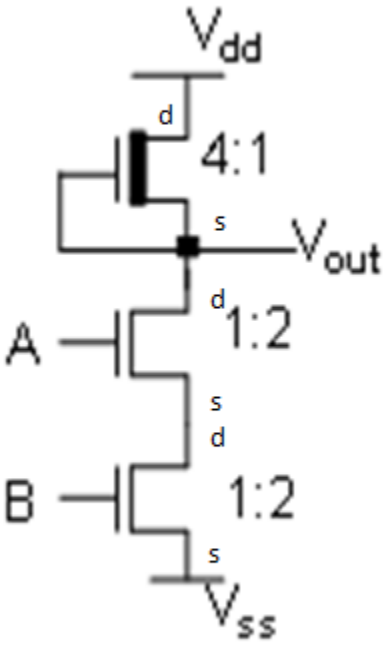
2 INPUT – CMOS NAND GATE



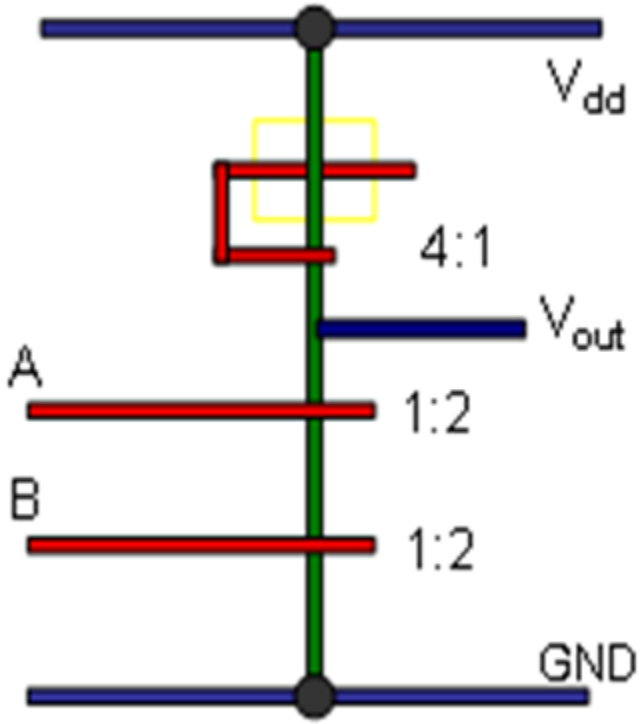
MASK LAYOUT –CMOS NAND GATE



Two input - Nmos NAND GATE

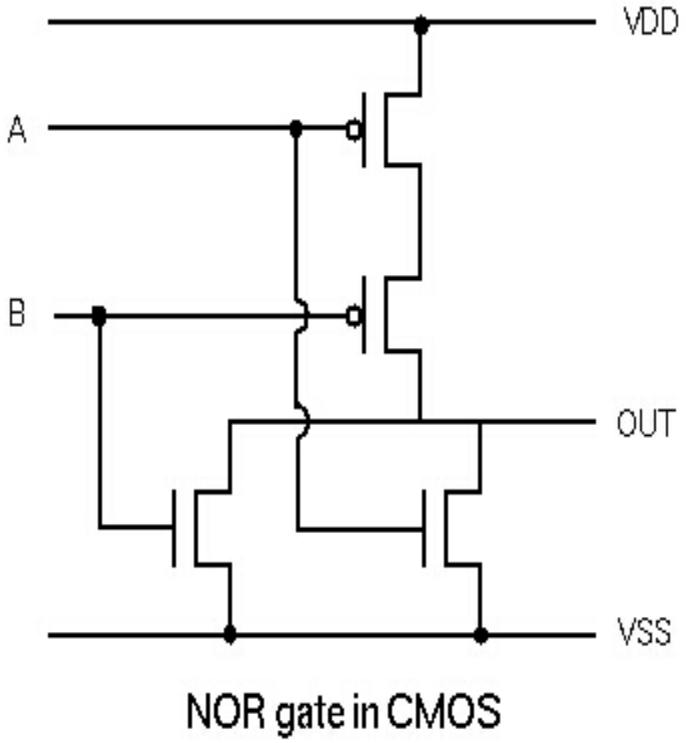


Schematic

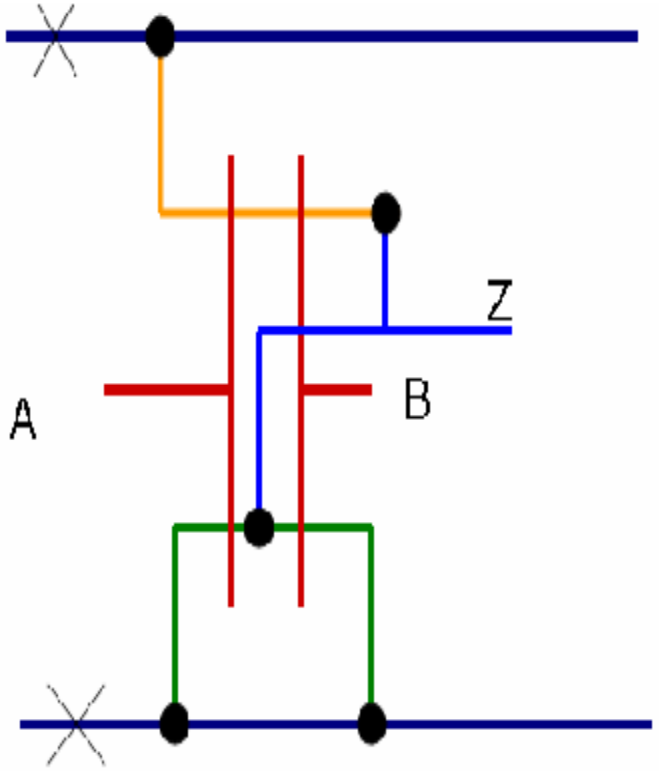


Stick diagram

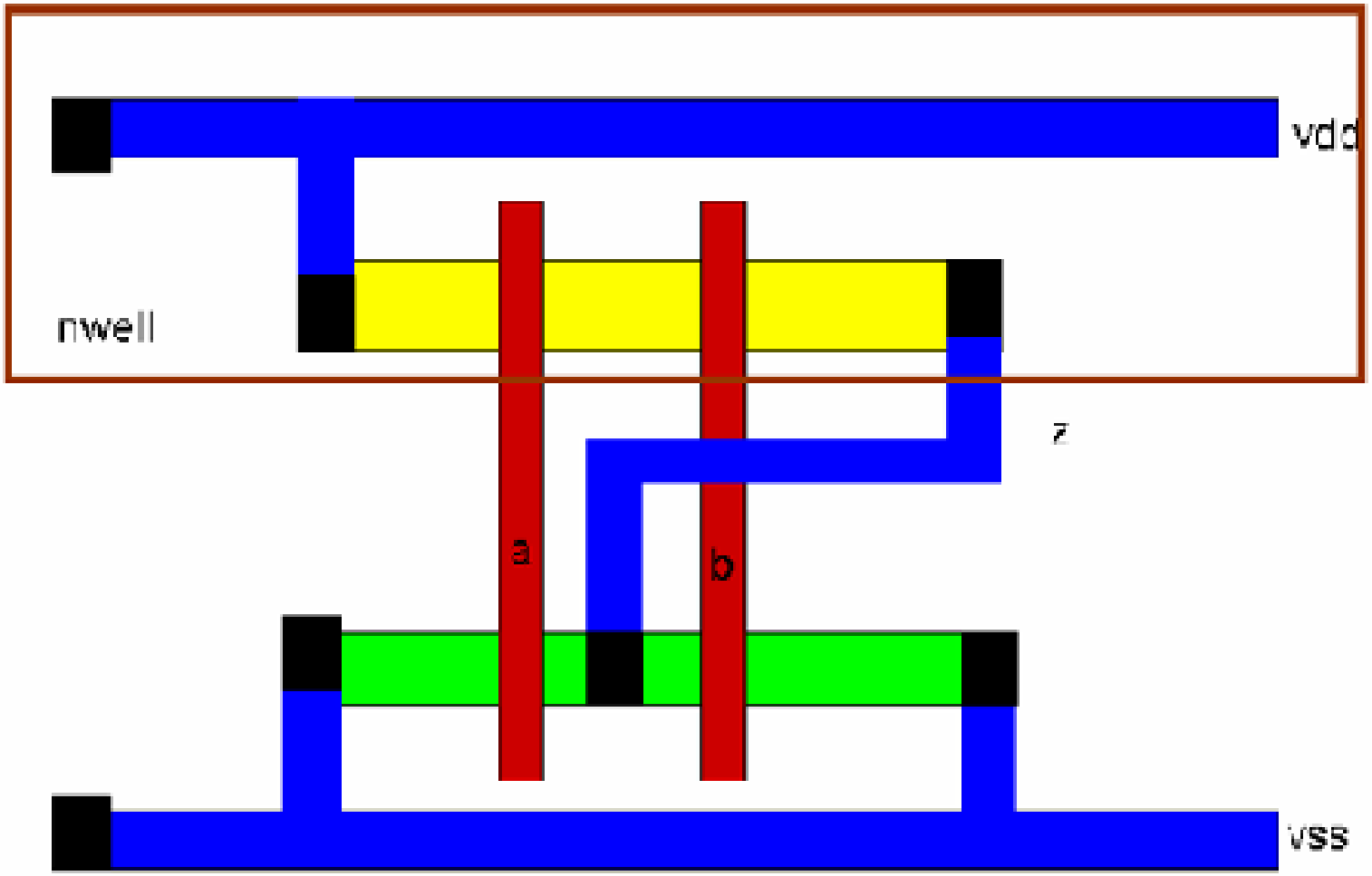
NOR gate



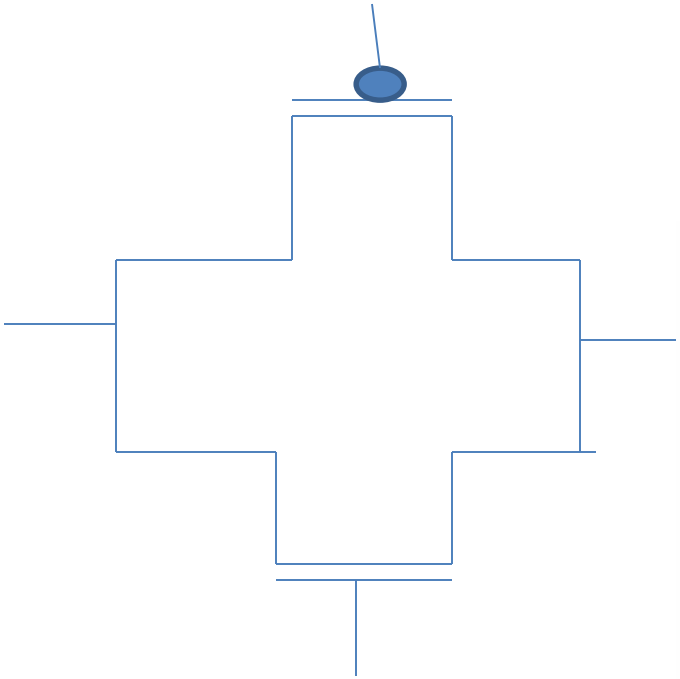
NOR gate in CMOS

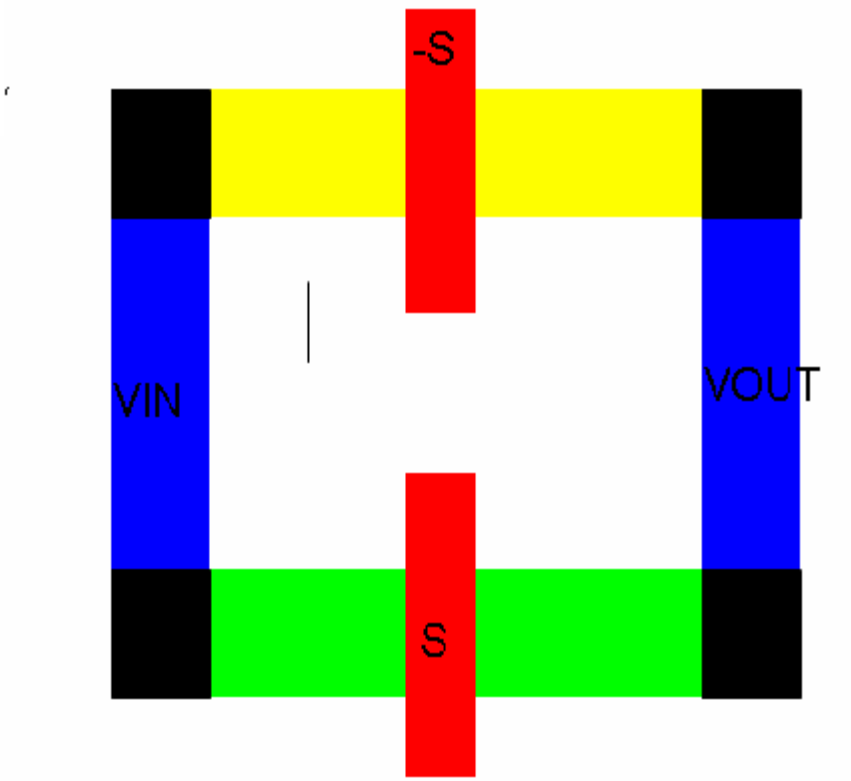


MASK LAYOUT –CMOS NOR GATE



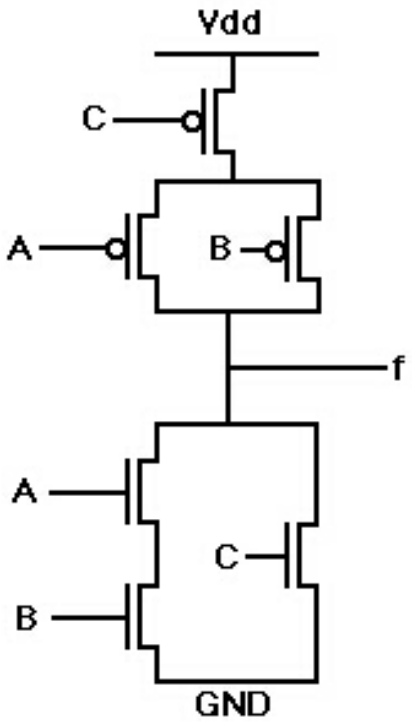
MASK LAYOUT

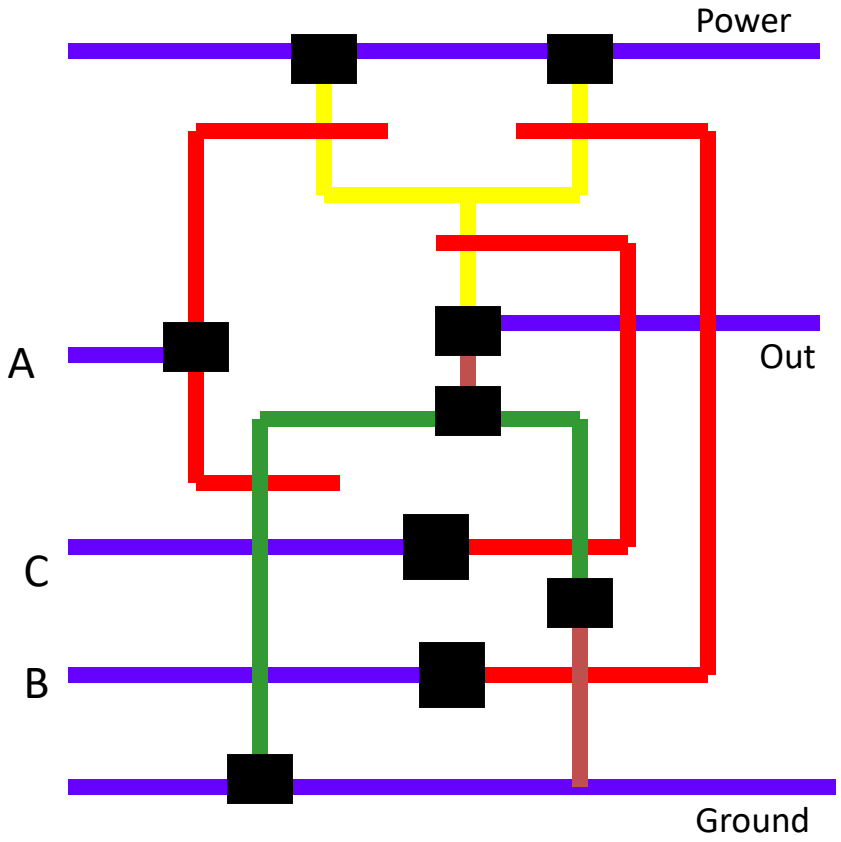




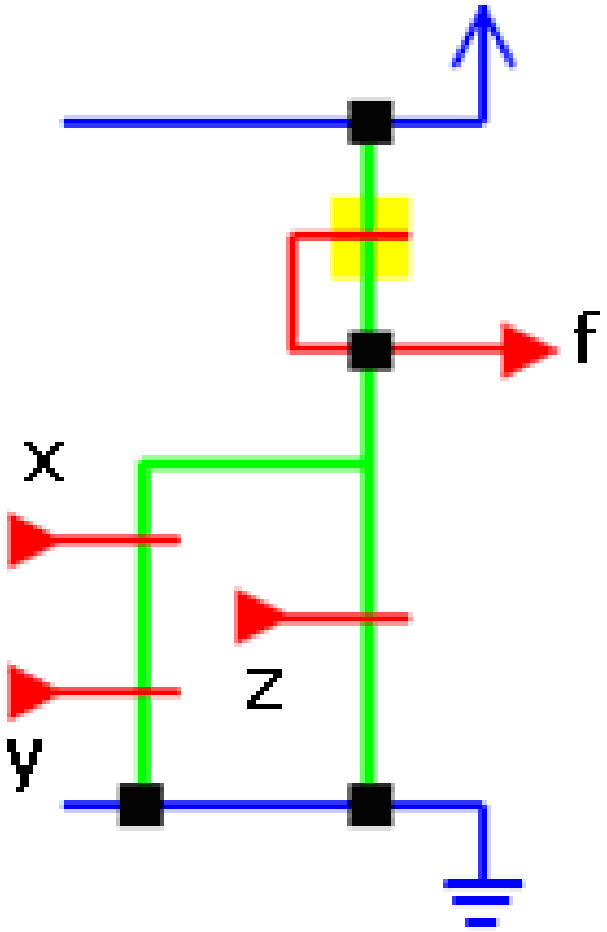
FUNCTION

Example: $f = \overline{(A \bullet B) + C}$

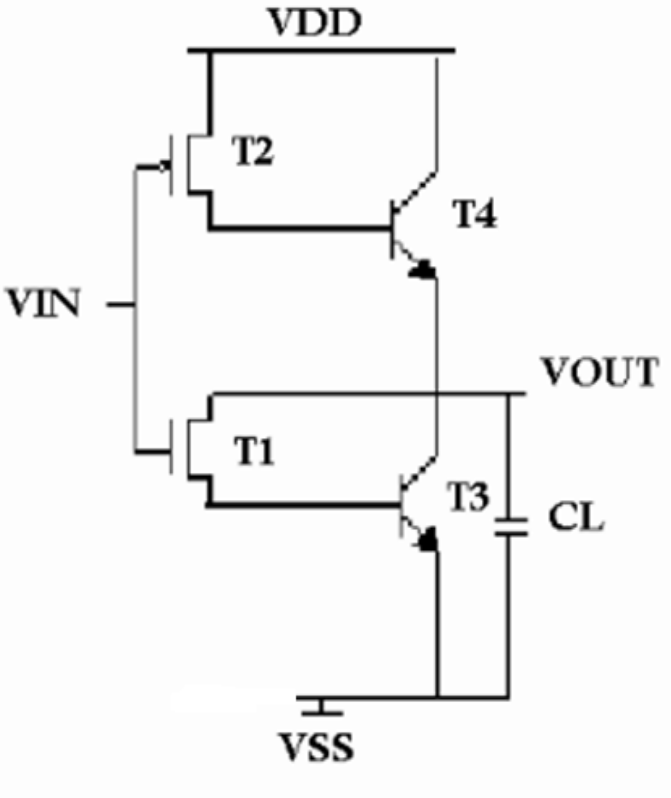


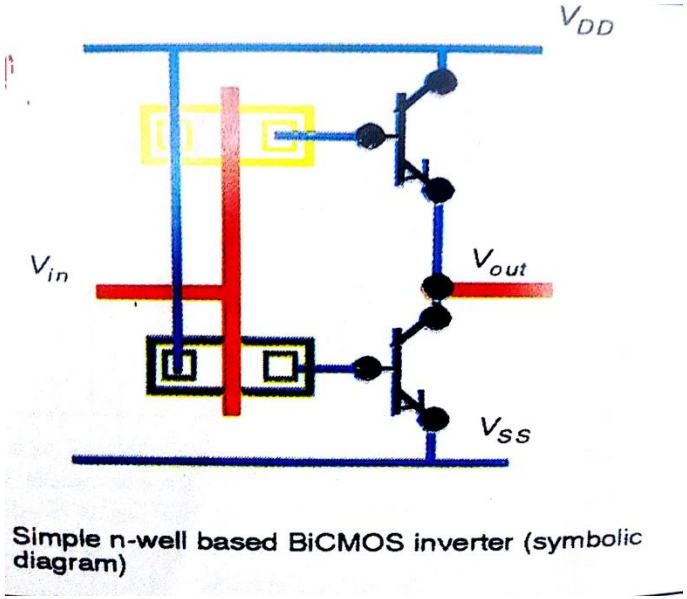


stick diagram nMOS implementation of the function f’ = [(x.y)+z]

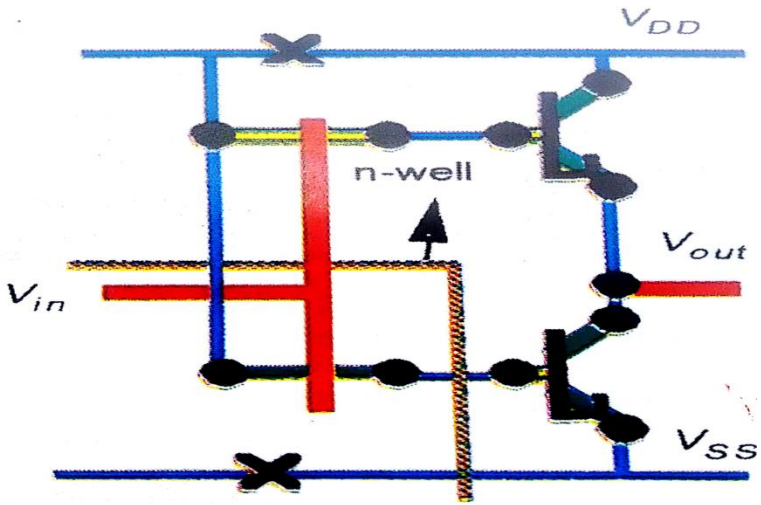


n-well Bi-CMOS inverter.



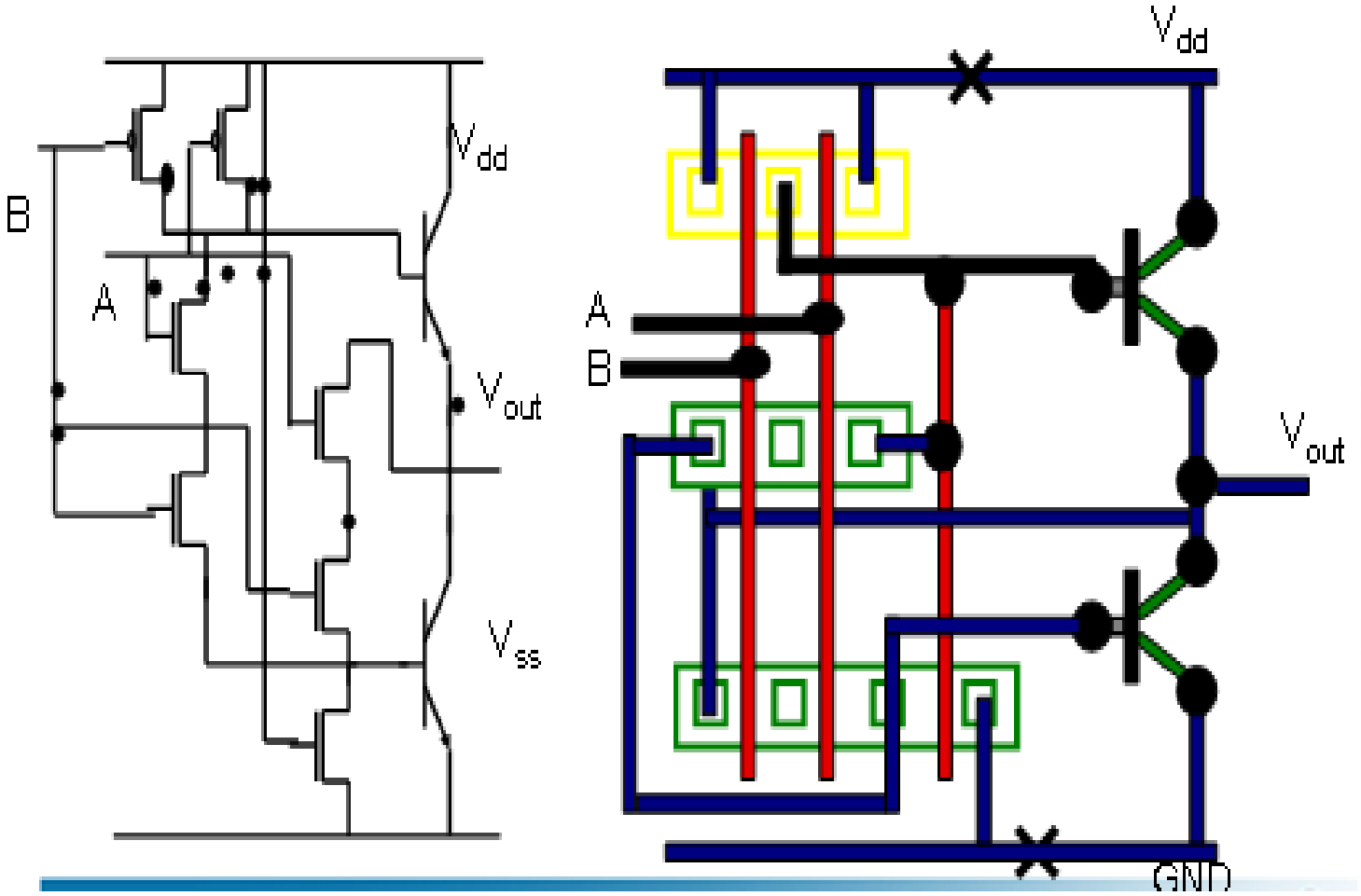


Simple n-well based BiCMOS inverter (symbolic diagram)



Simple n-well based BiCMOS inverter (stick diagram)

Bi –CMOS NAND gate



I bit cmos shift register

- Refer module -5 for stick diagram

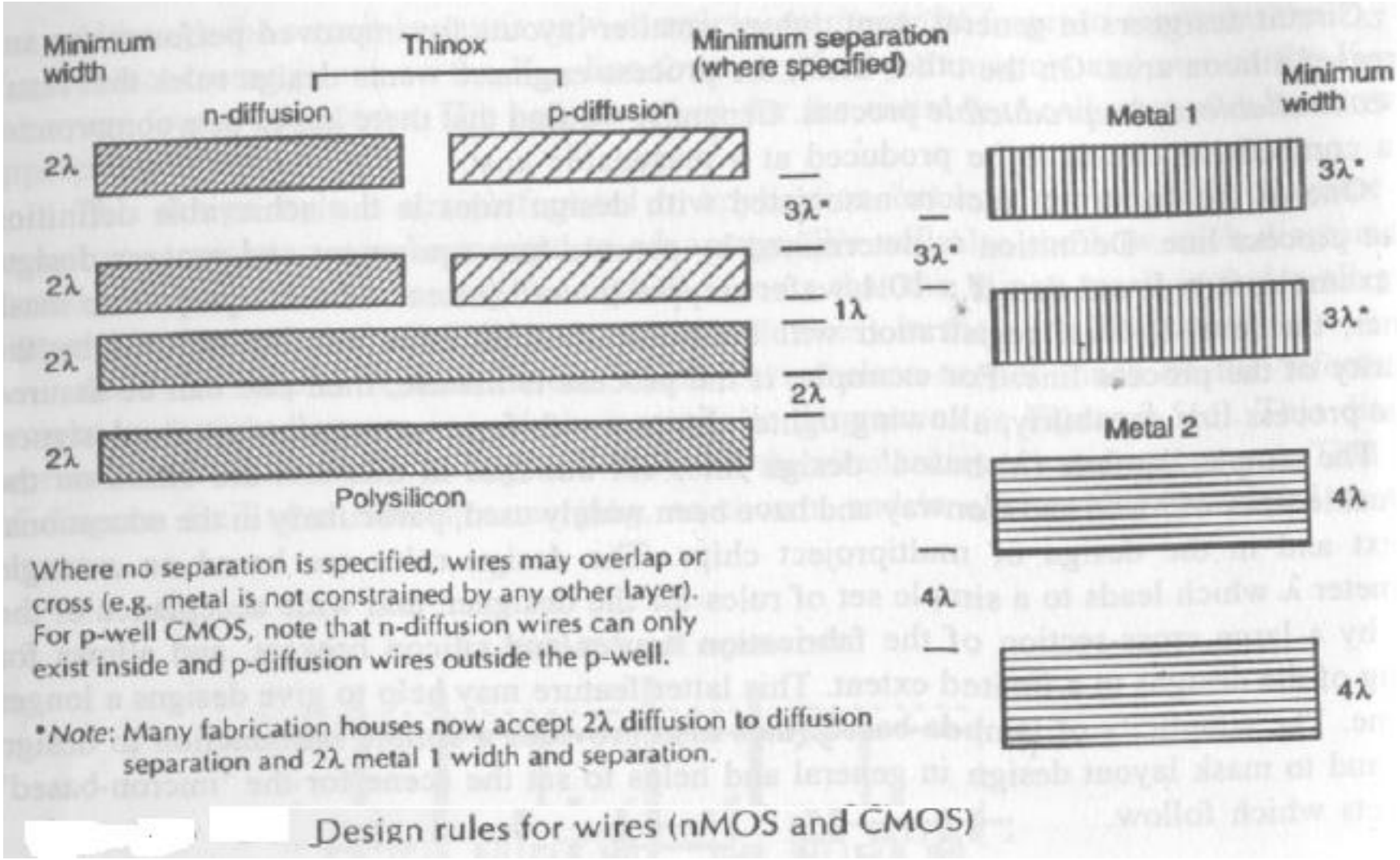
Design Rules

- Allow translation of circuits (usually in stick diagram or symbolic form) into actual geometry in silicon
- Interface between circuit designer and fabrication engineer
- Compromise
  - Circuit designer wants tighter, smaller layouts or improved performance.
  - Process engineer wants design rules that result in a controllable, reproducible process.
- Lambda based design rules – work of Mead and Conway – used widely.

Lambda Based Design Rules

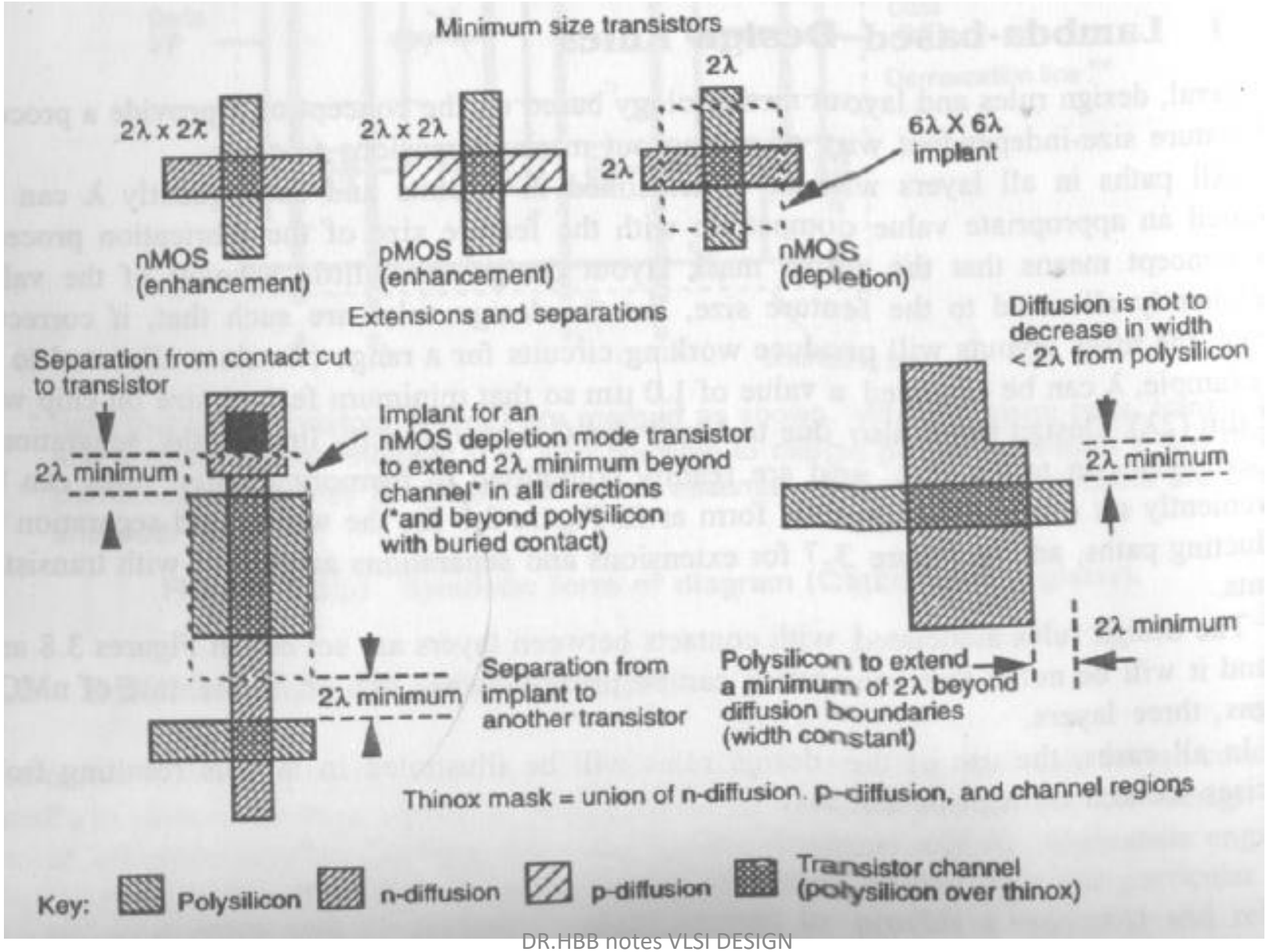
- Design rules based on single parameter, λ .
- Simple for the designer ,Widely accepted rule.
- Provide feature size independent way of setting out mask.
- If design rules are obeyed, masks will produce working circuits .
- Minimum feature size is defined as “2 λ”.
- All paths in all layers will be mentioned in “λ” units.
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

Design rules for the diffusion layers and metal layers

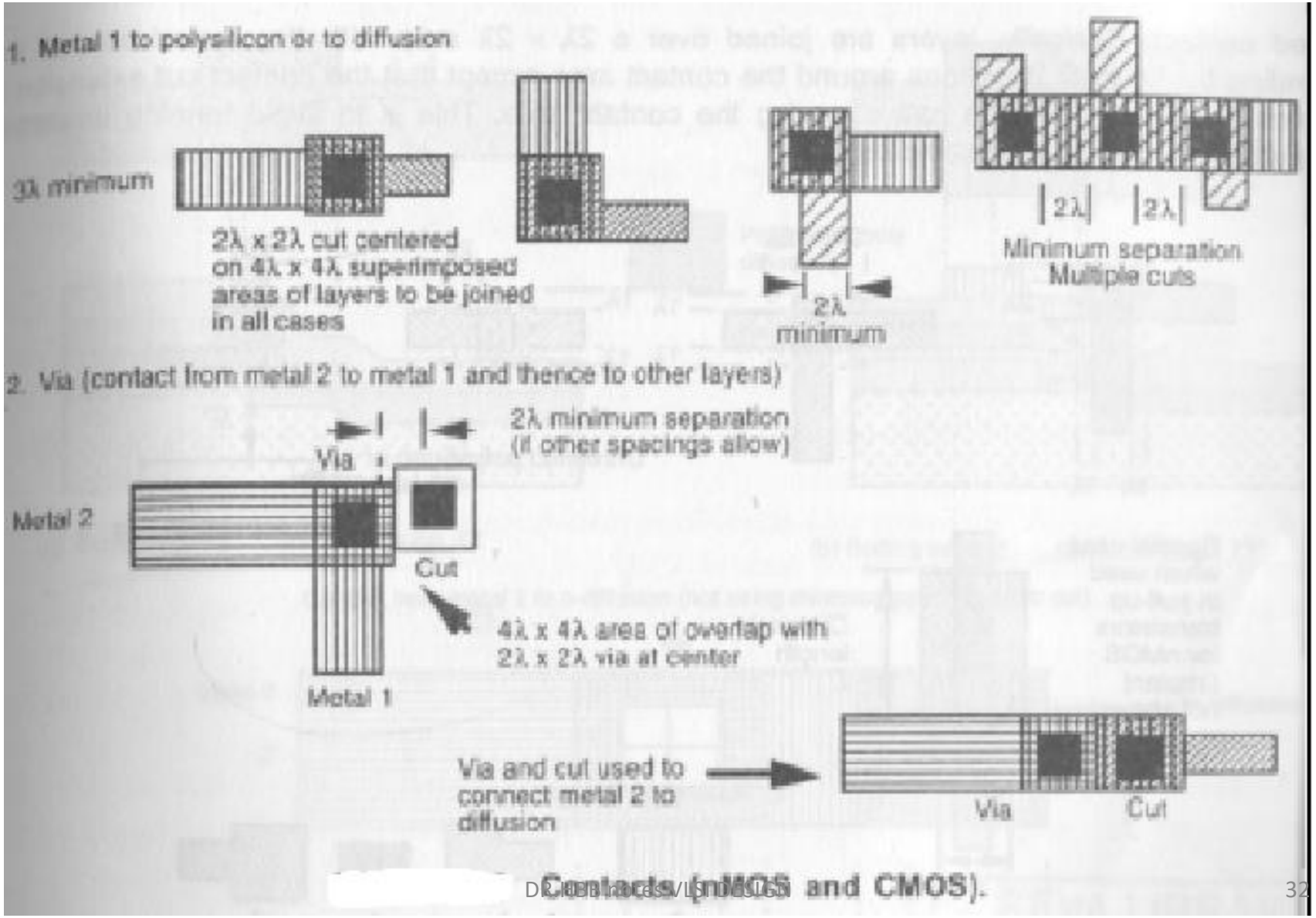


Design rules for wires (nMOS and CMOS)

Design rules for transistors



Contacts (nmos & CMOS)



Contacts (nMOS and CMOS).

Contact cuts: assignments for students 3.3.2 ,3.3.3,3.3.4

- When contacts are made b/w polysilicon and diffusion in ckts, we have 2 approaches.

  Buried contact and butting contact

Buried contact: no metal cap should be used to establish the contact.

Butting contact : Metallization is used to establish contact b/e the two.

What is Via?

It is used to connect higher level metals from metal1 connection.

The design rule for contact is minimum 2x2 and same is applicable for a Via.