Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering

Internship Program Report on "Chip Design Flow using Cadence"
Duration: 1 Month (8th July to 2nd August 2024)

Introduction

The Department of Electronics and Instrumentation Engineering at Shri Govindram Seksaria Institute of Technology and Science (SGSITS) successfully conducted a one-month internship program on "Chip Design Flow using Cadence ." The internship aimed to provide students with hands-on experience and industry insights into VLSI design methodologies using Cadence Virtuoso software tools. The program included expert talks and practical training sessions to enhance participants' understanding of the chip design process. About **40 students** took part in internship .The internship saw participation from students of various esteemed institutions, including **SVVV, IPS Academy, Oriental University, Acropolis Institute, and Prestige Institute.**

Objectives

We Aim:

- To familiarize students with the complete chip design flow.
- To provide hands-on experience with Cadence Virtuoso software tools.
- To expose students to industry best practices in VLSI design.
- To facilitate interaction with industry experts and academicians in the field.

Expert Talks

The internship program featured expert talks from distinguished professionals in the field of VLSI:

- **Mr. Neeraj Jain(Qualcomm Taiwan)** – Provided insights into front-end design methodologies and RTL coding techniques.
- **Mr. Himanshu Tiwari(Texas Instumentaion)** – Delivered a session on digital circuit design and synthesis techniques.
- **Mr. Preet Jain(professor SVVV University)** – Delivered a session on physical design, including floor planning, placement, and routing.
- **Dr. Vaibhav Neema(professor DAVV university)** – Discussed verification strategies, sign-off methodologies, and industry trends in chip design.
- **Dr. R.C. Gurjar (Associate Professor, SGSITS)** – Explained advanced VLSI design concepts and emerging trends in semiconductor technology.
- **Dr. Rajesh Khatri (Associate Professor, SGSITS)** – Provided insights into mixed-signal design and Analog layout techniques.

Curriculum and Training Modules
The internship was structured into multiple modules covering the following aspects:

Module 1: Introduction to VLSI and Cadence Virtuoso Tools

- Overview of VLSI design
- Introduction to Cadence Virtuoso software suite
- Setting up the design environment

Module 2: Simulation and analysis

- Functional simulation and debugging
- Analysis of Design Trends

Module 3: Back-End Design

- Layout Design
- Design rule check (DRC) and layout versus schematic (LVS) checks
- Parasitic Extraction

Module 4: Verification and Sign-Off

- Post layout Simulation and verification
- Final verification and tape-out procedures

Lab Sessions
In addition to expert talks, practical lab sessions were conducted by **Ms. Mansi Jain**, **Project Associate C2S**, where students worked on hands-on projects using Cadence Virtuoso software. The sessions covered:

- Setting up and running simulations.
- Layout design and verification.
- Implementation of basic digital circuits.
- Optimization techniques for efficient chip design.

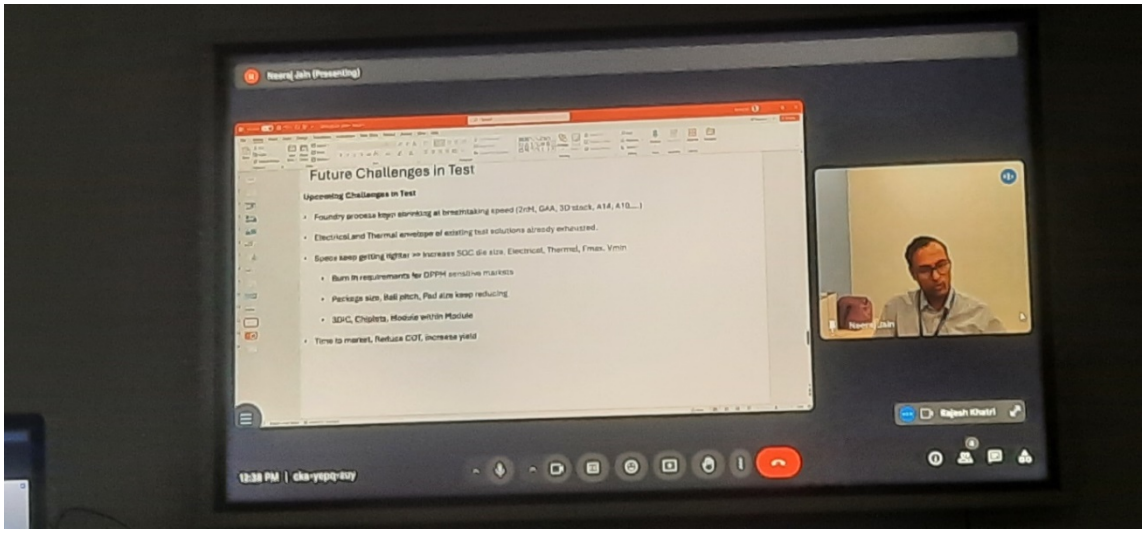
Conclusion

The one-month internship program on "Chip Design Flow using Cadence Virtuoso" was a highly enriching experience for all participants. The combination of theoretical sessions, hands-on training, and expert interactions provided a holistic understanding of the VLSI design process. The Department of Electronics and Instrumentation Engineering at SGSITS remains committed to organizing such initiatives to enhance students' technical competencies and industry readiness. We have taken the feedback and outcomes are as follows:

- Participants gained hands-on experience in designing and verifying digital circuits using industry-standard tools.
- The expert talks provided valuable industry insights, bridging the gap between academia and real-world applications.

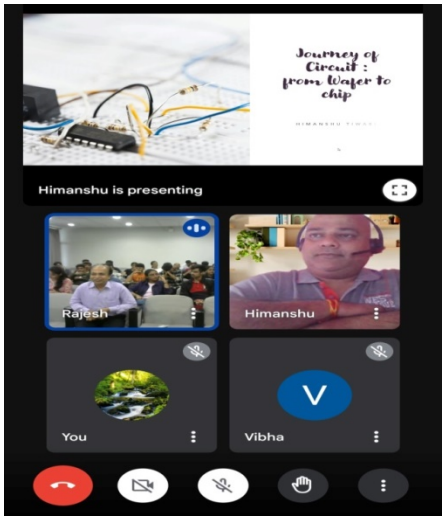
- Students developed essential skills required for careers in semiconductor design and VLSI industries.
- The program fostered collaboration and networking among students, faculty, and industry professionals

Flyer of Training Program



Expert talks by industry professional From Qualcomm Taiwan Mr Neeraj Jain

Expert talks by Academic professional From SVVV University Mr. Preet Jain



Expert talks by industry professional From Texas Instumentaion Banglore Mr. Himanshu Tiwari

Certificate distribution and concluding ceremony