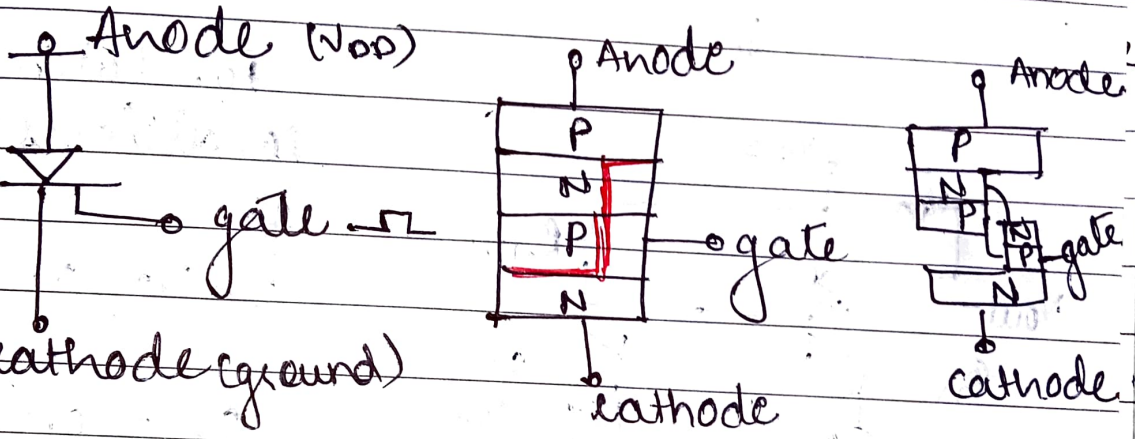
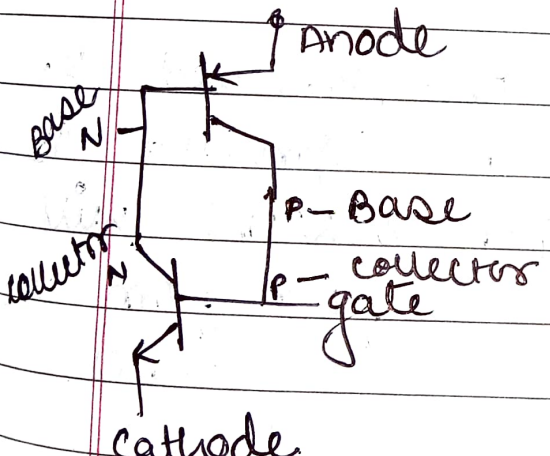
Latch up in CMOS

Unit-5

→ Generation of low impedance path in CMOS circuit b/w V_{DD} (supply) & ground.

→ so, high current will get driven by V_{DD} towards ground & that may damage in CMOS circuit

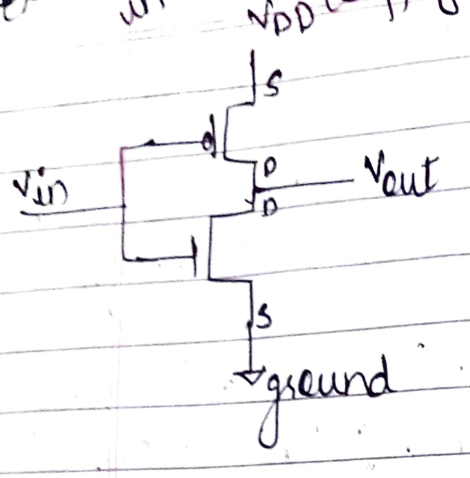




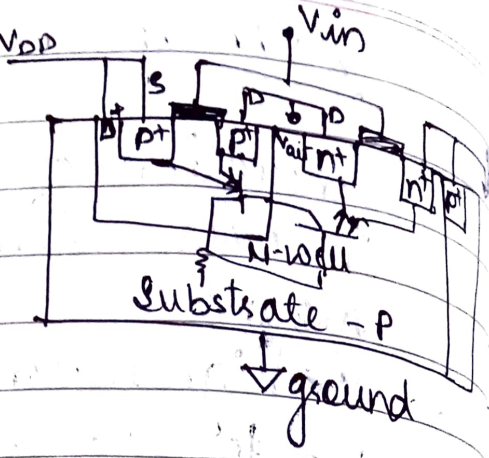
* forward bias
Anode - V_{DD}
cathode - ground
* gate ⊓ pulse
SCR - turned on

→ current will flow from V_{DD} to gnd even though remove gate pulse
cf Latch-up of SCR
→ same as in CMOS

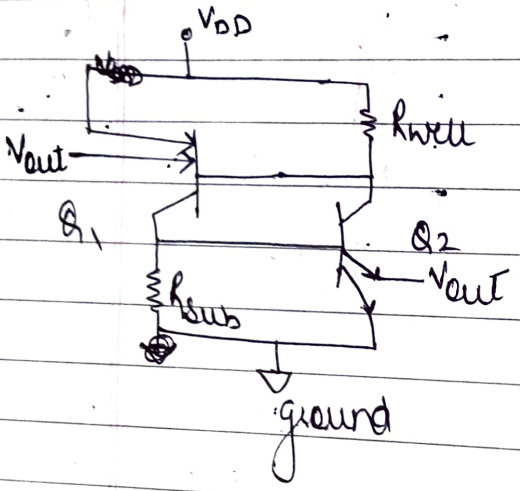
Example of inverter using CMOS



p^+/n^+ → substrate contact for PMOS & NMOS



equivalent ckt



multi emitter terminal

For Latch in CMOS conditions:

① if V_{in} or $V_{out} > V_{DD}$

Q_1 – on

EB - forward Q_1
BE – forward Q_2
then current will flow from V_{DD} to ground.

② if V_{in} or $V_{out} <$ ground

Q_2 – EB – forward – ON
Q_1 – forward – ON

regenerative feedback

→ retrograde well
→ P on P^+

Prevent latch-up steps

1. Add gold impurities in substrate, will minimize life time of minorities in transistor, that will reduce latch up
2. By providing epitaxial layer, can reduce (R_{sub}) substrate resistance.
3. ~~Substrate N-well as close placement~~ of substrate & well as close as possible
4. Avoide forward biasing of source & drain.
5. Place P-MOS close to V_{DD} & N-MOS close to ground