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Patent Search

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Abstract:

In this proposed work an ADC designed is completed with area efficient and low power consumption. After that detailed study of INL and DNL estimate and their error for 8 bit ADC. Error minimization for both INL, DNL and ENOB estimate shows effectiveness of algorithm for testing ADC using histogram technique. Ideal ADC transfer characteristic simulation is done and arbitrarily non linearity error is introduced. Extensive test and evaluation is done by doing simulation of 5 to 8 bit ADC character have incorporated estimation of error in DNL, INL and improvements in estimated DNL, INL and ENOB is reported.

Complete Specification

Claims:1. A new design and testing of a pipeline A/D converter (ADC) system for high speed data converting application , Description:Technical field

The present invention in general relates to a new design and testing of a pipeline A/D converter (ADC) system for high speed data converting application

Background of the invention:

ADC is an important device widely used in electronics, communication and instrumentation systems for interfacing analog electronics with digital electronics. All the methods are sophisticated, costly and time consuming, every people cannot effort. It is a dream of every young researchers and designer that if the method test the devices and determining the design parameters. In case of high volume production of Integrated Circuits (ICs), manufacturing costs are strongly affected by testing. Hence ADC design and testing is an important activity which plays main role in deciding accuracy of a system. I have proposed the software based a novel design and testing of a Pipeline A/D Converter (ADC) System for high speed data converting applications. This proposed design will be area efficient, low power consumption, time saver and user friendly.

Objective of the invention

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