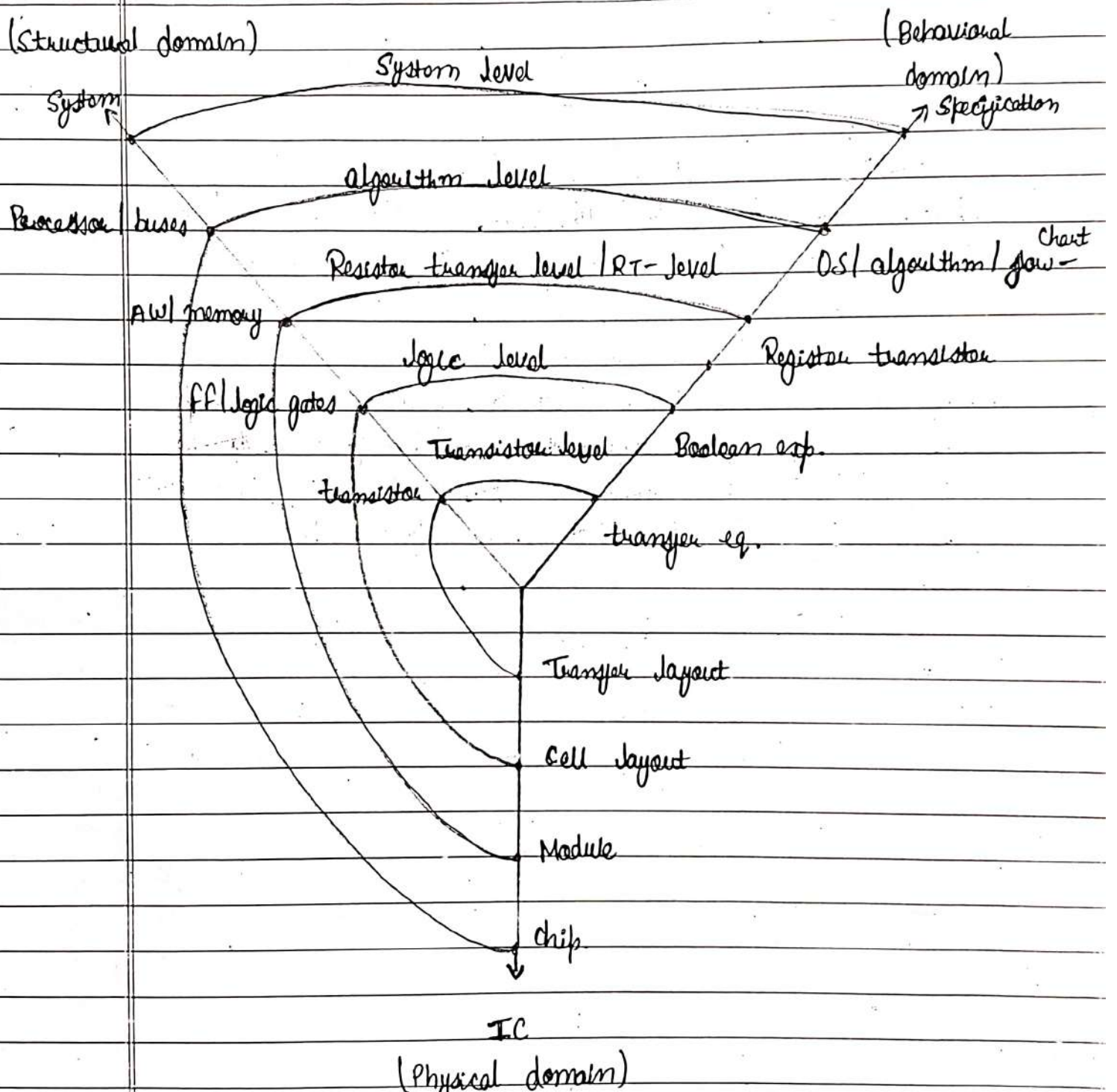
Navbodh
PAGE NO.:
DATE: / /

U-1

Q1→ Draw the Y- chart & explain all the domain of VLSI.

Ans)



शिक्षक के हस्ताक्षर : _____

प्रयोग क्र.: _____ दिनांक : _____

Behavioral domain :- It is created to analyze the design in terms of functionality, performance, compliance to given standards, & other specifications.

Structural domain :- A system is described in terms of subsystems. Here the diff subsystems & their interconnection to each other are listed for each level of abstraction.

Physical domain :- All IC's must be realized on a chip. The domain gives information on how the subparts can be seen in structural domain. There is information about the size, the shape & the physical placement.

शिक्षक के हस्ताक्षर : _____

Date: / / Page no:

The Y- chart consists of three major domains.
1. Behavioral domain
2. Structural domain
3. Geometrical layout domain

→ The design flow chart starts from the algorithm that describes the behavior of the target chip.
→ The corresponding architecture of the processor is first defined.
→ It is mapped onto the chip surface by floorplaning.
→ The next design evolution in the behavioral domain defines ~~infinite~~ finite state machines (FSM's) which are structurally implemented with functional modules such as registers & arithmatic logic units.
→ These modules are then geometrically placed onto the chip surface using CAD tools for automatic module placement followed by routing, with a goal of minimizing the interconnects area & signal delays.
→ The 3rd evolution starts with a behavioral module description. Individual modules are then implemented with leaf cells.
→ At this stage the chip is described in terms of logic gates (leaf cells), which can be placed & interconnected by using a cell placement & routine program.
→ The last evolution involves a detailed boolean description of leaf cells followed by a transistor level implementation of leaf cells & mask generation.

Date: / / Page no:

→ In standard cell based design, leaf cells are already pre-designed & stored in a library for logic design use.

- Explain Regularity, Modularity & locality.

1) Regularity :- Decomposition of a large system in simple and similar blocks as much as possible.
Ex :- Design of array structures consisting of identical cells such as parallel multiplication array.

2) Modularity :- In design means that the various functional blocks which make up the larger system must have well defined functions & interfaces.
→ It allows that each block or module can be designed relatively independently from each other.
→ All of the blocks can be combined with ease at the end of the design process, to form the large system.
→ The concept of modularity enables the parallelisation of the design process.

3) Locality :- The concept of locality also ensures that connections are mostly between neighbouring modules, avoiding long-distance connections as much as possible.

Navbodh
PAGE NO.:
DATE: / /

Q2 (1) What do you mean by abstraction level.

Ans) It could be defined as the amount of information an entity is hiding within it.

Level of abstraction :-
- System level
- Chip level
- Register level
- Gate level
- Circuit level
- Layout level

↓ less detailed

↓ more detailed

(2) VLSI design flow | Design hierarchy.

[System verification]

function design

↓

function Verification

↓

logic design

↓

logic Verification

↓

Circuit design

↓

Circuit Verification

↓

Physical design

↓

Physical Verification

शिक्षक के हस्ताक्षर :

- Hierarchical design.
  - Top-down design.
    - → The initial work is quite abstract & theoretical & there is no direct connection to silicon until many steps have been completed.
    - → Acceptable in modern digital system design.
    - → Co-design with combining HW/SW is critical.
    - → Similar to cell-based design flow.
  - ~~Top~~-Bottom-up design.
    - → Start at the silicon or circuit level & builds primitive units such as logic gates, adders & registers as the first step.
    - → Acceptable for small projects
    - → Similar to full-custom design flow.

Date : Page :

- Explanation of VLSI design flow.

1) System Spec's :- It is high level representation of the system. The factors to be considered in this process include peyormance, functionality & interface.

2) Architectural design :- Design engineer design the architecture according to system Spec's.

3) Functional Verification :- Functionality of design are identified. It specify the hardware implementation of system functionality. The outcome of functional design is usually a timing diagram.

4) Logic design :- In this, register allocation, logic & arithmatic operations of the design that represent the functional design are derived & tested this description is called RTL description. In this step, System ~~Verification~~ Spec's is expressed in hardware description language such as Verilog & VHDL.

5) Logic Verification :- To Verify whether the Synthesis tool has correctly generated the gate-level netlist a Verification should be done.

6) Circuit design :- In this step circuit is designed based on the logic design. The boolean expressions are converted into circuit representation by taking into consideration the power & speed requirement of original design.

7) Circuit Verification :- It is used to Verify the correctness & timing of each component. Dig. consists circuit elements such as gates & transistors.

Date : Page :

8] Physical design :- The netlist is converted into physical geometric representation. Layout is representation of an IC in terms of planar geometric shapes which ~~corresponding~~ correspond to the patterns of metal oxide or Semiconductor layers that make up the components of the integrated circuit.

9] Physical Verification :- We perform it to check such as layout Vs schematic (LVS) & design rule check (DRC). ~~DER~~ DRC Verifies whether the given layout satisfies the design rules provided by the fabrication team. LVS is a major check. Layout is compared with the Schematic for verifying whether their functionally match or not.

Navbodh
PAGE NO.:
DATE: / /

Q5 → Discuss the physical design in details.

Ans) 1. Partitioning :- It can be done in the RTL design phase. When the design engineer partitions the entire design into sub-blocks & then proceeds to design each module.

2. Floorplanning :- It determines the size, shape & locations of modules in a chip & as such it estimates the total chip area, the interconnects & delay. Computationally, VLSI floorplanning is an NP hard problems.

3. Placement :- Placement is the process of finding a suitable physical location for each cell in the block. It does not just place the standard cell available in the synthesized netlist, it also optimized the design. It will be driven based on diff criteria like timing driven, congestion driven, power optimization.

4. Routing :- Making physical connections bet signal pins using metal layers are called routing. Routing is the stage after CTS & optimization where exact paths for the interconnections of standard cells & macros & I/P pins are determined.

शिक्षक के हस्ताक्षर : _____

प्रयोग क्र.: _____ दिनांक : _____

Q1 (1) → front-end and back-end tools.
Ans→ Front-end :- Xilinx, altera.

Back-end :- Synopsis, cadence.

(2) → Merits & demerits of full custom & semicustom design.
Ans

Full custom :-

Merits	Demerits.
(A) Compact designs	Very time consuming
(B) Improved electrical characteristics.	More error prone.

Semi Custom :-

Merits	Demerits.
(A) Well tested standard cells which can be shared between users.	Can be time consuming to built-up standard cells.
(B) Good for bottom-up design.	Expensive in the short term.

शिक्षक के हस्ताक्षर : _____

Q → Diff bet Full & Semi Custom

	Full	Semi
1]	All mask layers are customized in full custom design.	– Uses pre designed logic cell (gates, mux) known as Std cell.
2]	Layouts are designed specifically. Design doesn't use pre-tested cells.	– Widely used, more cost, low – programmance.
3]	Less cost, high perfor	– Design time & complex less.
4]	Design time more, complexity more.	– Designer uses pre-tested cell.
5]	µP.	– Digital logics.

Date: / / Page no:

- Modelling

It plays a significant role in the efficient simulation of VLSI circuits. By simplifying the models used to analyze these circuits, it is possible to perform transient analyses with reasonable accuracy at speeds of one or two orders of magnitude faster than in conventional circuit simulation programs.

Types :-

(1) Gate-level modeling
(2) Data flow modeling
(3) Behavioral modeling
(4) Mixed design style modeling

- Simulation

It plays an important role in the design of integrated circuits. Using it, a designer can determine both the functionality and the performance of a design before the expensive and time-consuming step of manufacture.

Types :-

(1) Discrete event simulation
(2) Dynamic simulation
(3) Process simulation

- Synthesis / logic Synthesis.

It is in VLSI is the process of converting your program into a circuit. In terms of logic gates, Synthesis is the process of translating an abstract design into a properly implemented chip.

Types :-

(1) logical Synthesis
(2) Physical Synthesis

Synthesis Step :-

(1) Translation
(2) logic optimization
(3) Gate level mapping
(4) Final optimization.

Q → Front-end & backend tools used in VLSI.

F.E. = Xilinx

B.E. = Cadence

Date : Page :

- VLSI design styles.

1) Field- programmable gate array :

→ fully fabricated IC chip in which the interconnections can be programmed to implement different functions.

→ Has thousand of logic gates to implement any logic function.

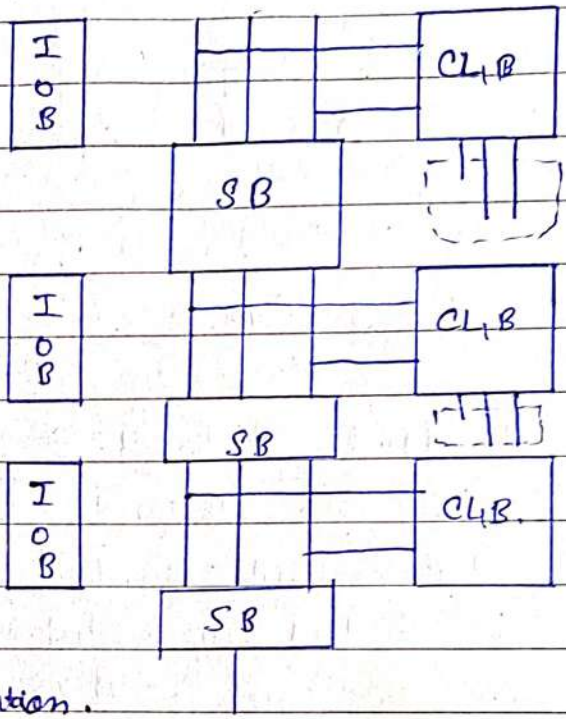
→ Three main components are :-

1) I/O buffer

2) Array of CLB's

3) Programmable interconnects

→ Used for fast prototyping, cost efficiency chip design especially for low volume application.



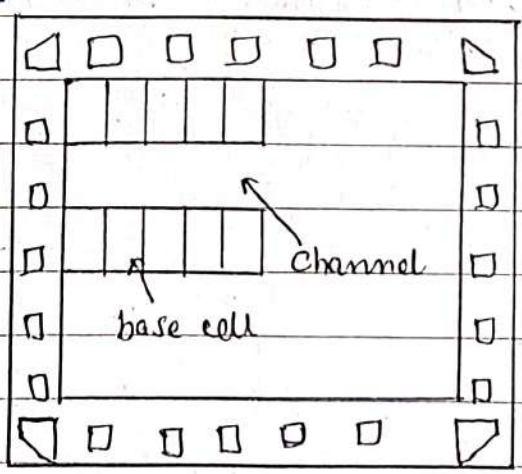
2) Gate Array design.

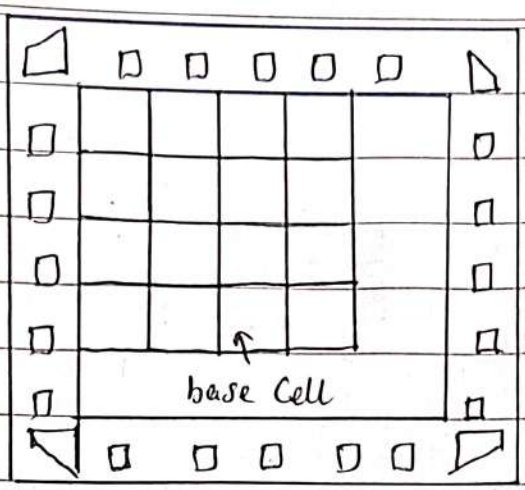
→ The transistors are fabricated in the silicon wafer but the interconnects are not fabricated.

→ The metal mask layers are customized to define the interconnections bet. the transistors for a targeted functionality.

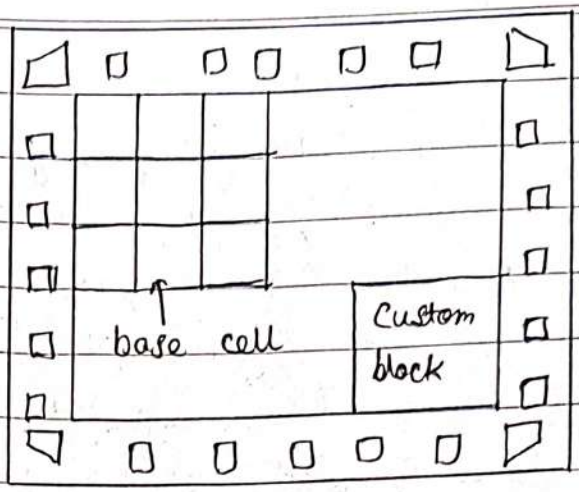
Three types of GAD :-

(A) Channelled.





(b) Channel- less.



(c) Structured

3] Standard cell based design.

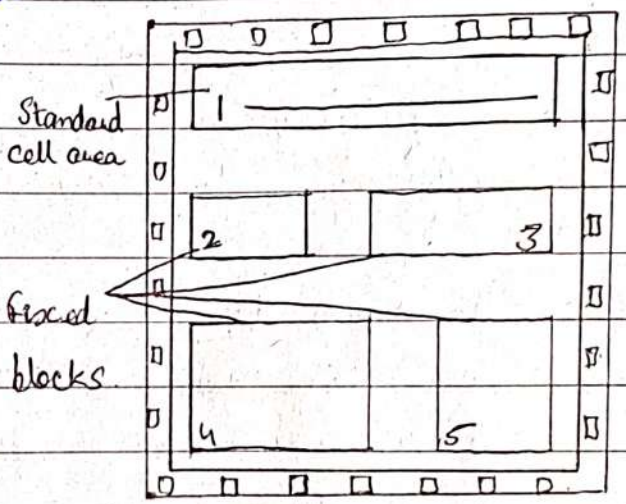
→ Uses the pre- designed, pre- tested & characterized standard cells.

→ The standard cells includes basic logic gates such as AND, OR, NAND, etc.

→ Some mega cells such as multiplexer, full adder, decoder, etc.

→ Sequential elements such as D-ff, register etc.

→ I/o buffer and some special cells.



→ All these standard cells are designed, tested & characterized & put it in a database, called standard cell library.

Date : Page :

4] full custom design.

→ Designers do not used pre-designed standard cell library. Instead, they design the entire chip from the scratch.

→ As each & every parts are designed. The chips are highly optimized for area, power & delay.

→ Superior to any other design style.

→ But cycle time is very high compared to other design.

5] Semi Custom design.

→ Almost all the basic building blocks are used from the standard library.

→ Only few cells are designed from the beginning which are not available in the standard cell library or to be optimized for a specific target.

→ This approach is faster compared to full custom design but slower than standard cell based design.

→ Peformance wise it is better than standard cell based design but inferior to the full custom design.

Date : Page :

Parameters	Full	Semi	FPGA.
1. Time to market	max	< >	min
2. Cost	max (if fabricating single)	< >	min.
3. Performance	best (ASIC)	in b/w	not feasible
4. Area	min	in b/w	max.