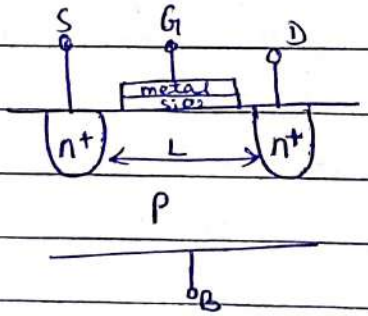
Unit 3 : Basics of CMOS:

Operation of NMOS, PMOS, CMOS, Bi CMOS, VCT, power dissipation, speed, area.
CMOS logic structure: domino logic, NP zipper logic, CVSL, DVSL.

→ CMOS - complementary mosfet
widely use to form ckts in numerous & varied application
low power dissipation
relatively high speed
high noise margin
Operate in wide range of source & IP voltage.

MOSFET : metal oxide semiconductor feeld effect transistor.

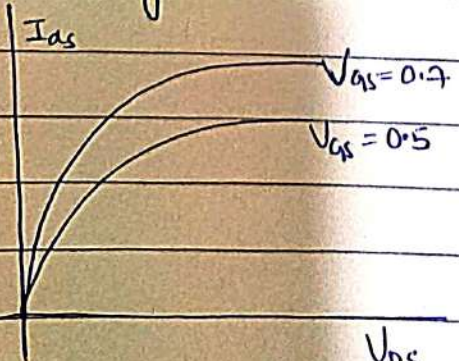
MOS :-



$$I_d = \frac{1}{2} K_n \left(\frac{W}{L}\right)(V_{gs} - V_t)^2$$

nowadays we use polysilicon at metal instead of aluminium.

Characteristics:



(the W/L in Id is design variable)
L is channel length.
Sometimes gate length is nearly same.
W: width of MOS

CMOS are found in many electronic components including microprocessor batteries, digital camera image sensor

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$K_n = \mu_n C_{ox}\left(\frac{W}{L}\right)$ μ_n = mobility of e^- we can't control

C_{ox} : oxide capacitance $\frac{\varepsilon_{ox}}{t_{ox}}$

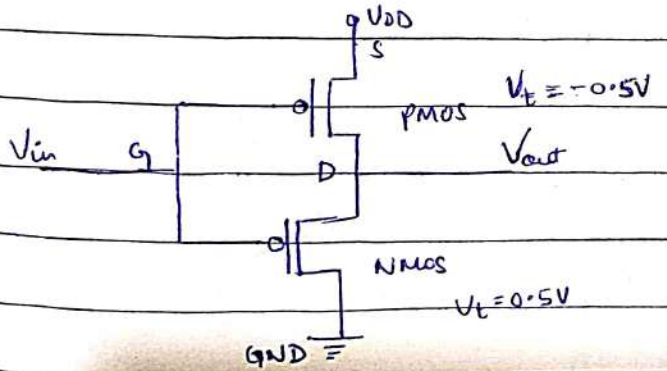
The main problem with MOS is that it acts as capacitor, & if we want fast switching ckt then value of R×C should be minimum. Any capacitance consists of two conductive plates filled with dielectric.

CMOS inverter :- combining complementary & symmetrical pair of p-type & n-type MOSFETs to create logic functions

one p-type & one n-type MOSFET are wired together to make complementary symmetrical pair.

p-type : low resistance b/w source & drain when low voltage applied at gate

n-type : high resistance

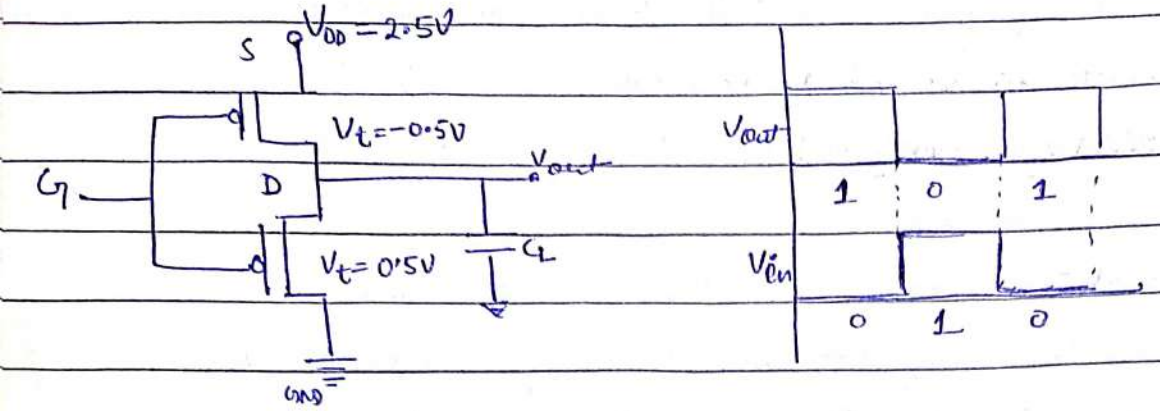


under static condition power drawn by CMOS inverter is 0 or negligible.

no direct path exists b/w the supply voltage and ground in static condition.

When we have NMOS, then the threshold is going to be some +ve value as we need to create a channel. The V_{GS} is used to determine whether the NMOS is in ON state or NOT.

$V_{GS})_n > V_t$ here V_t is threshold voltage.



fan out: how many CMOS unit we can connect with V_{out} of previous.
Ideally the number is ∞ but practically there is some leakage.

full swing is parameter which determines max achievable O/P voltage & min achievable O/P voltage.

There is problem with CMOS called latching problem (latch up) & another is more no. of transistors

for PMOS $V_{DSP} \geq V_{GSP} - V_{tn}$

for NMOS $V_{DSP} \leq V_{GSP} - V_{tp}$

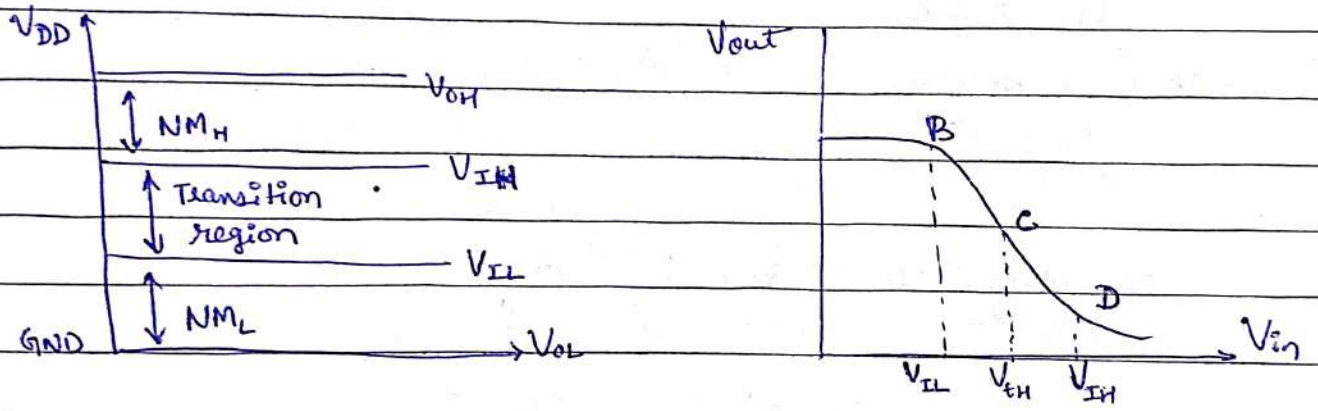
When $V_{in} = 1$ NMOS – on PMOS – off C_L charging
$V_{in} = 0$ NMOS – off PMOS – on

→ $V_{out} = 2.5$ current across PMOS will be drawn when V_{out} will be less than 2.5 due to potential diff.
When capacitor was charging current will be drawn if capacitor is fully charged no current will be drawn.

Advantages of CMOS inverter :-

→ under static condition power ≃ 0 (power drawn by CMOS is nearly 0)
→ No direct path exists b/w supply & ground in static cond^n.
→ VTC resembles with ideal inverter curve.
→ large noise tolerance
→ low power consumption
→ full o/p swing (max equal to supply voltage & min = ground level)
→ ideally ∞ no of fanout can be connected to CMOS inverter further

Noise Margin :-

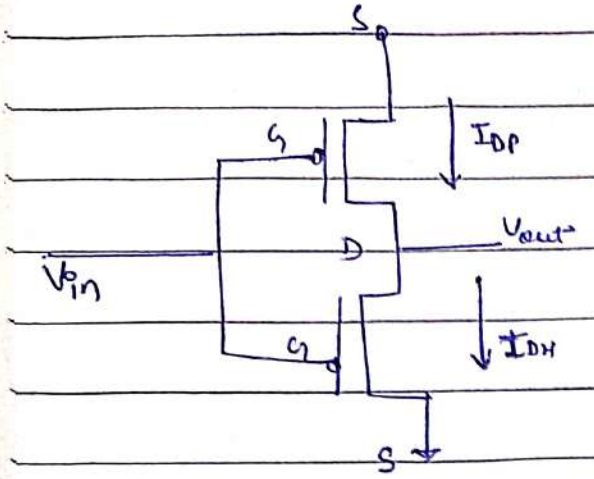


Noise margin is the range which is tolerable to CMOS such that the o/p is not impacted.

here noise = voltage in brief : It is total amt of acceptable V.

$$NM_L = V_{IL} - V_{OL}$$

V_{DD} is also written, but not equal to V_{OH} becoz there might be some voltage drop across PMOS.



Let NMOS be in Saturation region
PMOS be in linear region

$$I_{dn} = \frac{1}{2} K_n (V_{GSn} - V_{tn})^2$$

$$I_{dp} = K_p \left[(V_{GSp} - V_{to}) V_{DSp} - \frac{1}{2} V_{DSp}^2 \right]$$

equating both of them

$$I_{dn} = I_{dp}$$

$$\frac{1}{2} K_n [V_{in} - V_{tn}]^2 = K_p \left[(V_{in} - V_{DD} - V_{tp})(V_{out} - V_{DD}) - \frac{1}{2} (V_{out} - V_{DD})^2 \right]$$

$$K_n [V_{in} - V_{tn}] = K_p \left[\left(\frac{dV_{in}}{dV_{in}} - 0 - 0 \right)(V_{out} - V_{DD}) + \left(\frac{dV_{out}}{dV_{in}} - 0 \right)(V_{in} - V_{DD} - V_{to}) - \frac{1}{2} \times 2 (V_{out} - V_{DD}) \frac{dV_{out}}{dV_{in}} \right]$$

$$K_n [V_{in} - V_{tn}] = K_p \left[(V_{out} - V_{dd}) + \frac{dV_{out}}{dV_{in}} (V_{in} - V_{DD} - V_{to}) - (V_{out} - V_{DD}) \frac{dV_{out}}{\partial V_{in}} \right]$$

Assuming $\frac{dV_{out}}{dV_{in}} = 1$ (slope).

$$\frac{K_n}{K_p} (V_{in} - V_{tn}) = \left[V_{out} - V_{dd} + V_{in} + V_{DD} + V_{to} + V_{out} + V_{DD} \right]$$

$K_n / K_p = K_r$

$$K_R V_{in} + V_{in} = 2V_{out} - V_{dd} + V_{tp} + V_{tn} K_R$$

$$V_{in} = \left[\frac{2V_{out} - V_{dd} + V_{tp} + K_R V_{tn}}{1 + K_R}\right]$$

$$V_{in} = V_{IL}$$

$$\boxed{V_{IL} = \frac{2V_{out} - V_{DD} + V_{tp} + K_R V_{tn}}{1 + K_R}}$$

$$K_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n$$

$$K_R = \frac{\mu_n C_{ox} (W/L)_n}{\mu_p C_{ox} (W/L)_p} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$V_{IH} = \frac{V_{DD} + V_{top} + K_R(2V_{out} + V_{ton})}{1 + K_R}$$

$$V_{th} = \frac{V_{ton} + \sqrt{\frac{1}{K_R}}(V_{DD} + V_{top})}{1 + \sqrt{\frac{1}{K_R}}}$$

V_{IH} → minimum I/P voltage which can be interpreted as logic 1.

V_{IL} → max I/P voltage which can be interpreted as logic 0.

Ideally V_{OH} should be equal to supply V_{DD} & $V_{OL} = 0$ if there is no drop.

$NM_H = V_{OH} - V_{IH}$ // high noise margin

$NM_L = V_{OL} - V_{IL}$ // low noise margin

if not mentioned $V_{OH} \approx V_{DD}$ & $V_{OL} \approx GND$.

* Power dissipation across CMOS inverter :—

→ static power dissipation (P_{dc})

→ dynamic power dissipation (P_{dyn})

→ short ckt power loss (P_{sc})

$$P_{diss} = P_{dc} + P_{dyn} + P_{sc}$$

$$P_{dc} = I_o \left(e^{V/nV_T} - 1\right) V_{DD} \simeq 0$$

<u>dynamic power dissipation</u> :— due to switching activity

when I/P goes from 0 → 1 the PMOS gets off & NMOS acts as discharging path & power is dissipated through it.

Dynamic power dissipation is due to charging & discharging of capacitor.

$$P_{dynamic} = \frac{1}{T} \int_0^T V(t)\, i(t)\, dt$$

$$= \frac{1}{T} \int_0^T V_{out}\, C_L \frac{dV}{dt}\, dt$$

When charging is done +ve else −ve

$$= \frac{1}{T} \int_0^{T/2} V_{out} \left(-C_L \frac{dV_{out}}{dt}\right) dt$$

↙ discharging

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for charging: $\frac{1}{T}\int_{T/2}^{T}(V_{DD}-V_{out})\left(C_L\frac{dV_{out}}{dt}\right)dt$ $V=(V_{DD}-V_{out})$ → Vi across PMOS

Adding both.

$$\frac{1}{T}C_L\left[-\int_0^{T/2}V_{out}\,dV_{out}\,dt+\int_{T/2}^{T}(V_{DD}-V_{out})\,dV_{out}\right]$$

$$\frac{1}{T}C_L\left[\left[\frac{-V_{out}^2}{2}\right]_0^{T/2}+\left[\frac{2V_{DD}V_{out}-V_{out}^2}{2}\right]_{T/2}^{T}\right]$$

at $T=0$ $V_{out}=V_{DD}$

$T/2$ $V_{out}=0$

$T=T$ $V_{out}=V_{DD}$

$$\frac{1}{T}C_L\left[\frac{-1}{2}(-V_{DD})^2+V_{DD}(V_{DD}-0)-\left(\frac{V_{dd}^2}{2}-0\right)\right]$$

$$\frac{1}{T}C_L\left[\frac{V_{DD}^2}{2}+V_{DD}^2-\frac{V_{DD}^2}{2}\right]$$

$$\frac{1}{T}C_L V_{DD}^2$$

$$P_{dynamic}=fC_LV_{DD}^2$$