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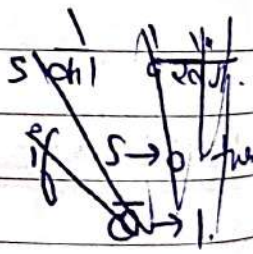
U-4.

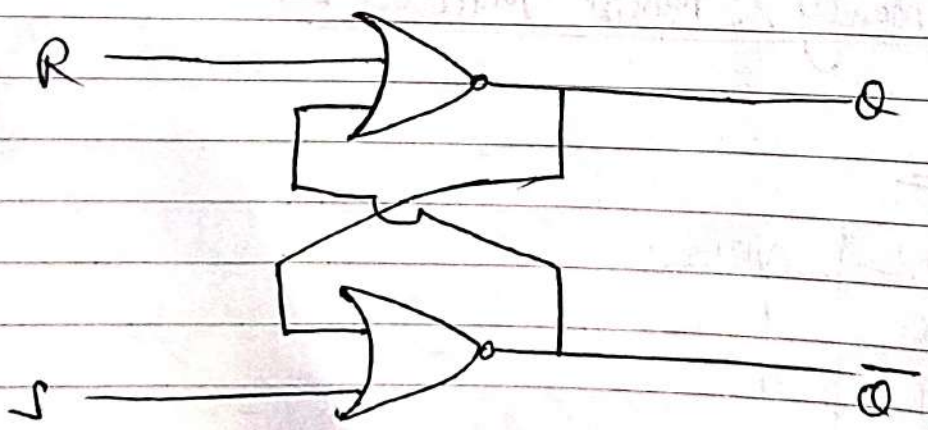
Basics of VLSI Design.
implementation of logic functions.
rise time / fall time / delay time considerations.
Fan-in, Fan-out, standard cell design,
cell libraries.
ASICs : various types
design flow
packaging & testing.

CMOS logic design ~~circuit~~ :-

(i) Z=

CMOS SR latch using NOR gates :-





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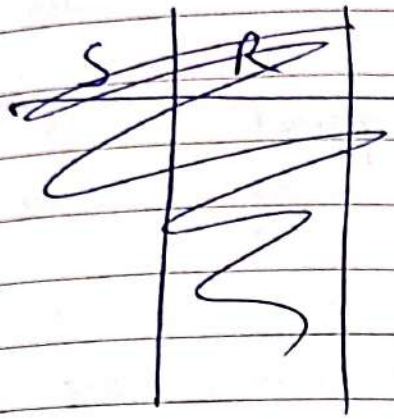

S	R	Q	$\bar{Q}$	Operation.
0	0	Memory.		Hold pov data.
0	1	0	1.	Reset.
1	0	1	0.	Set.
1	1	0	0.	Not allowed.

① $S \to 0$, $R \to 1$.

(Q → 0 क्यों NOR, opposite कर देता है sign को, Q feedback with S (0,0) → 1 देगा o/p. $\bar{Q}$).

② $S \to 1$, $R \to 0$.

($\bar{Q} \to 0$, ($\bar{Q}=0$ will go in feedback with R(0). तो o/p → 1 at Q).

③ $S \to 0$, $R \to 0$.

(Q(0), $\bar{Q}(0)$ o/p is not changing, we are holding the data where Q, $\bar{Q}$ works as memory.).

④ $S \to 1$, $R \to 1$.

(Not desired (0) आएगा).

o/p should be complement to each other.

pull up network.
pull down network.

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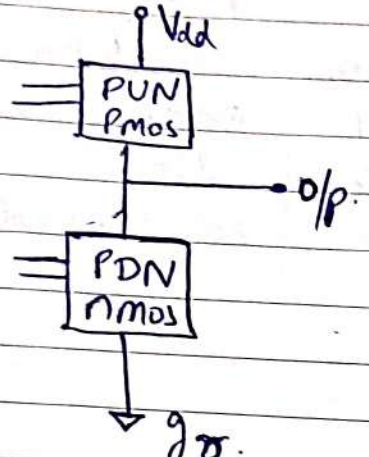
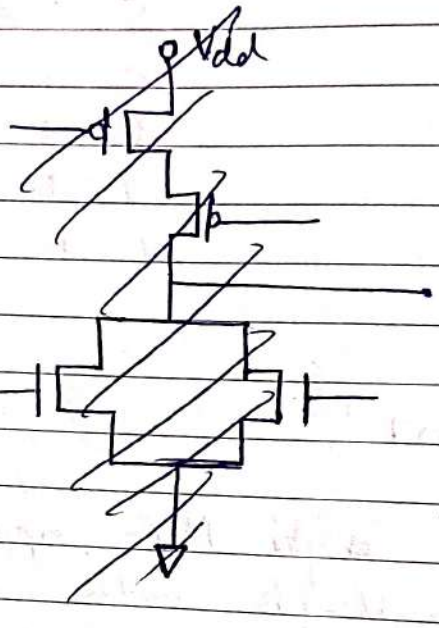
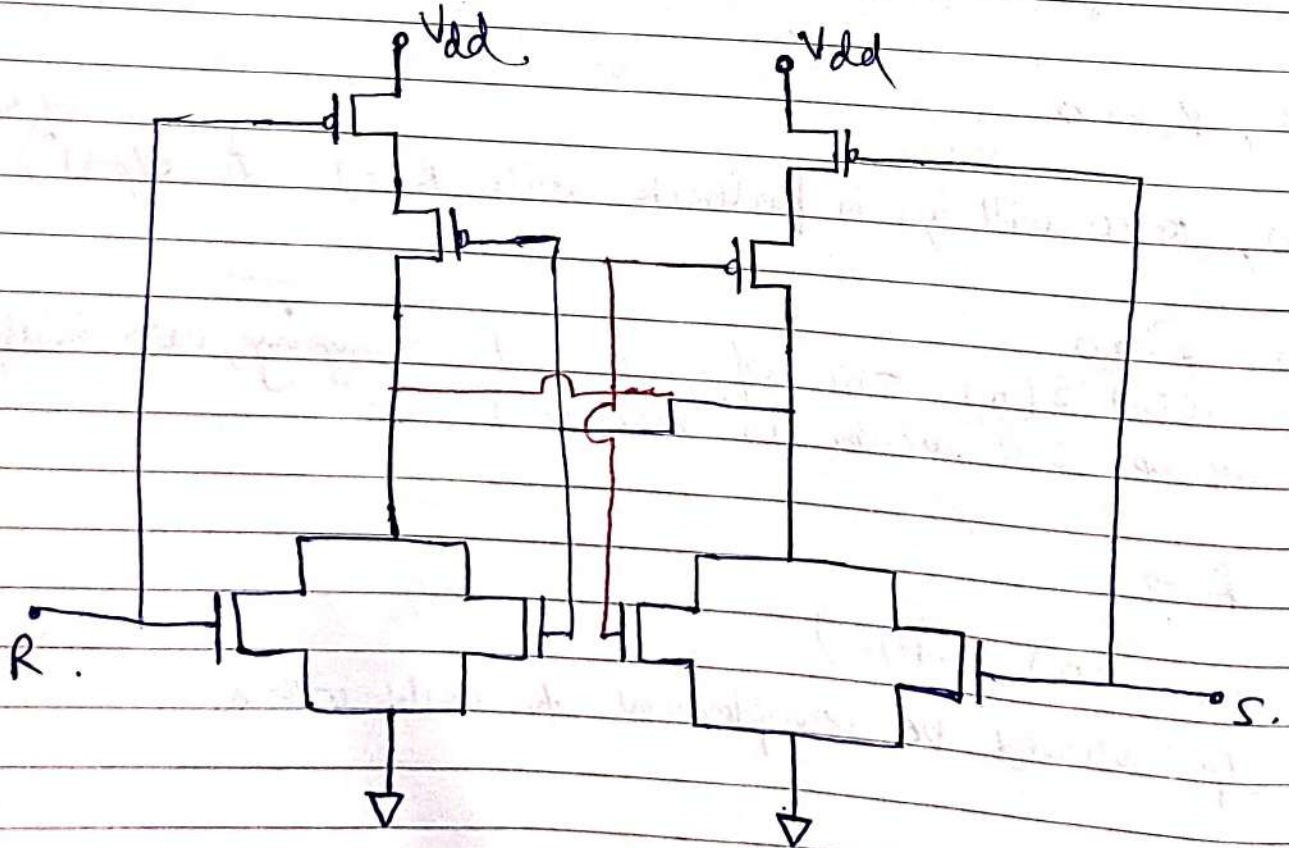
CMOS circuit

→ (+) operation → pmos – series → NMOS – parallel.







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Rise
~~Fall~~ time & fall time.

(t_r) → Rise time is the time, during transition, when output switches from 10% to 90% of the maximum values.

(t_f) → fall time is the time, during transition, when o/p switches from 90% to 10% of the maximum value.

~~Gate Array~~.

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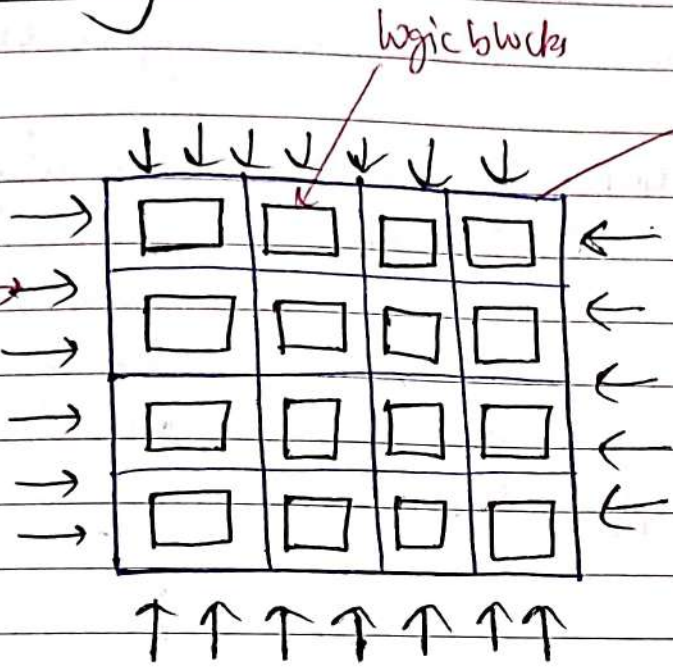
Gate Array →



→ Transistor level masking is fully defined.
→ Program wiring & via to implement the desired fn.
→ we take die which have all the gates placed but not connected.
→ only layout of interconnect is given to fabrication house.

● A Gate array circuit is a prefabricated circuit with no particular fn, in which transistors & other active devices are placed at regular predefined positions.

Advantage
→ Reduce the mask cost
→ less time to market.

dis.
→ size is fixed
→ No. of transistor are fixed
→ low efficiency.
→ suitable for lower production.

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ASIC → ASIC is an integrated circuit customized for a particular use or application.

ASIC is a combination of analog function (clock, amplification, noise suppressing), digital function (adder, mux, registers, CPU), programmable logic, different types of memory, power management in a single chip. so here chip is dedicated for a particular application.

Types.

① Semi-custom → It uses predesigned logic cell (AND, OR, FLOPS etc). known as standard cell. The ASIC & designer uses all these standard cell stored in the form of library & does placement of these cells & interconnection. All these cells are predesigned & so fully optimized. This semi custom design reduces design time & risks. can also change the transistor size here.

② Full-custom → here the designers design some or all the logic cell, circuit or layout, interconnection of its own for a specific application.

Its costly, time consuming but provide max performance, minimized area & highest flexibility as designed with our efforts.

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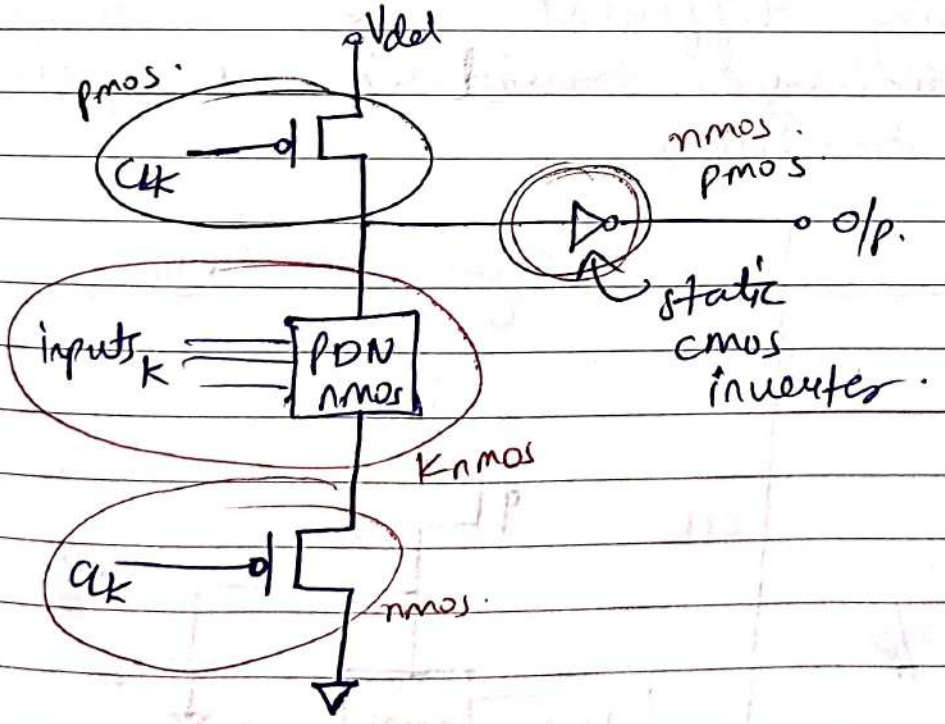
(3) Programmable ASIC → fPGA, PLD.

Domino logic CMOS →

In static CMOS, we use PDN made up of pmos. As pmos have more size, higher load capacitance & slower switching speed, we use dynamic CMOS.

→ But if we use dynamic CMOS, there are issues of cascading.

→ Soln to cascading pblm can be done by domino CMOS.



nmos → K+1+1
→ K+2
pmos → 1+1
→ 2.

DCVSL → Differential cascade voltage switch logic is a differential styles derived from conventional CMOS logic & satioed pseudo NMOS logic. It combines their advantages & provide a high speed, area efficient, & rail-to-rail logic design alternative.

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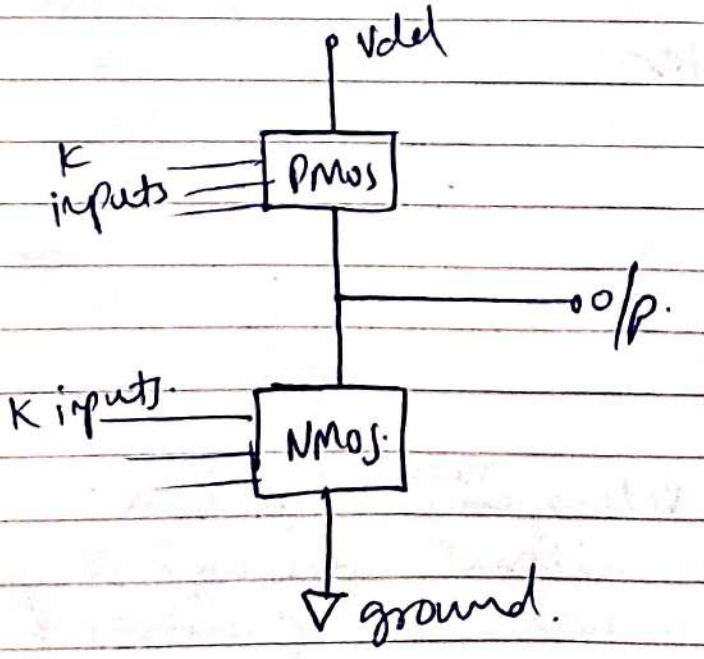
Pseudo NMOS → logic uses only one PMOS device as a pull-up device for a multi-transistor N-logic block. The used PMOS device has its gate connected to ground & is therefore always "ON".

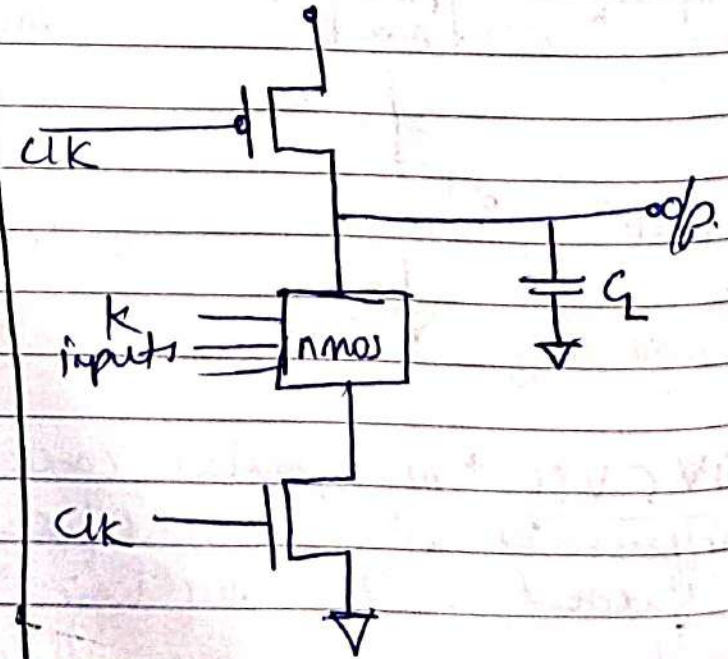
NP Domino logic → Domino logic is a system design style that eliminates the nMOS-nMOS glitch problem without introducing pMOS-type logic stages.

NP zipper logic → zipper logic is a scheme for improving charge leakage & charge sharing problems. It receives a slightly different clock signals for the pre-charge (discharge) transistors & for pull down (pull up) transistors.

Static CMOS



Dynamic CMOS



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→ nmos = K pmos = K.	→ nmos = |K+1| pmos = 1.
→ due to pmos overall size is more	→ due to only one pmos overall size is less.
→ due to more pmos, capacitive loading is more.	→ due to less pmos, capacitive loading is less.
→ No cascading issues	→ In cascading, some issues.
→ No need of pre charge for operation.	→ Re-charge of load C_L is reqd for dynamic CMOS operation.
→ No charge leakage	→ charge leakage creates problems.