DEVENDRA SINGH AJNAR

1. Personal Information			
(i)	Name	Devendra Singh Ajnar	**Photo** 
(ii)	Qualification	M.E.	
(iii)	Designation	Associate professor	
(iv)	Email-id	ajnards@gmail.com	
(v)	Employee No.	3300244	
(Vi)	Department	Electronics and Instrumentation	
(vii)	Experience	26 YRS	

2. Educational Qualification

S. No.	Degree	Specialization	Year	University/Board
1	M.E.	Electronics (DTI)	2003	RGPV BHOPAL
2	B.E.	Electronics and Telecommunication	1993	DAVV

3. Research Interests

VLSI, ACTIVE FILTERS

4. Research Paper Publications

(I) International/National Journal Publications

Design of 32 tap finite impulse response filter using Vedic multiplier and KoggeStone Adder
International journal of recent technology and engineering. IJRTE
ISSN 2277-3878 volume -8 issue-2 July 19 page no 6138-6141

(II) International/National Conference Publications
.FPGA implementation of quantum comparator using reversible logic (springer international conference-ICSCT 2019)Hyderabad .India **.Design and Simulation of two stage sample and hold circuit with low power using current conveyor** **.4th international conference on communication and electronics systems, July 2019 Coimbatore. India** **IEEE sponsored**

5. List of Conferences/Workshops/Seminars Organized
Advisory committee member in short term course on advancements in microelectronics and VLSI design .sponsored by tequip-3 (11th-15th march 2019) **Dept. E&I ,sgsits indore**

6. Invited Lectures/Expert Talks/Chairmanships at Conferences
GUEST SPEAKER (IETE CHEPTER) Designing analogue filter 8 August 2016,MIT Mandsaur