DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 1ST SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69002
SUBJECT NOMENCLATURE: DESIGN OF INTEGRATED CIRCUITS

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
4	-	-	4	-	-	CW	END SEM	SW	END SEM	
						30	70	-	-	100

Pre-Requisite: Knowledge of basic MOS Theory

Course Outcomes:

CO1: Understand MOS transistor theory and short channel effects.
CO2: Calculate Noise Margins & Propagation Delay of CMOS Inverter.
CO3: Analyze the combinational CMOS circuit for speed, power & area.
CO4: Implement combinational & sequential CMOS circuit with various topologies like domino logic, PTL etc.
CO5: Design of memories with efficient architectures to improve access times, power consumption
CO6: Understand EDA tool design flow for digital IC design.

Course Content:

Theory:

UNIT-I
Review of MOS transistor theory: Structure and Operation of MOS transistor, threshold voltage, First-order current-voltage characteristics, Short-channel MOS transistor, Short channel effects: Drain punch-through, DIBL, Hot carrier effect, Tunneling, Velocity saturation. Derivation of velocity saturated Current equation for short channel transistor, Alpha-Power law model, Sub-threshold conduction Body effect, channel length modulation, Capacitances of MOS transistor.

UNIT-II
MOS Inverter circuits: Introduction, Noise margin definitions, Voltage transfer characteristics (VTC), Calculations of various logic levels (V_{IL}, V_{OL}, VIH, VOH), threshold voltage of Inverter, Resistive load inverter, CMOS inverter, Pseudo-nMOS inverter, Dependence of VTC on W/L ratio, Transistor sizing, Inverter Dynamic characteristics: calculations of t_{plh} and t_{phl}, t_r, t_f and delay, Layout and design criteria, Stick diagrams.

UNIT-III
Static MOS Gate circuits: Introduction, CMOS gate circuits, basic CMOS gate sizing, fan-in and fan-out considerations, VTC of CMOS gates, Complex CMOS gates, XOR and XNOR gates, Multiplier circuits, Flip-flops and Latches, Power Dissipation in CMOS gates: Static, Dynamic, Power and Delay trade-offs.

UNIT-IV

High-Speed CMOS and Dynamic Logic Design: Switching time analysis, Gate sizing with velocity saturation effect, load capacitance calculations, Gate sizing for optimal path delay, inverter chain optimization, logical effort, optimizing path with logical effort. Dynamic logic design-Pass transistor logic, transmission gate logic, Domino logic, charge sharing, NP Zipper logic etc.

UNIT-V

Semiconductor Memory Design: Introduction, Memory organization,, types, MOS decoders, Static RAM cell design, DRAM cell design, three-transistor and one transistor dynamic cell Flash memoryFRAMS.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Principles of CMOS VLSI Design- Neil Weste and Kamran Eshraghain
2. Digital Integrated Circuits- Rabaey, Chandrakasan.
3. CMOS Digital Integrated Circuits- Kang, Leblebici.

Reference Book:

1. Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology – David Hodges, Horace Jackson and Rasve Saleh.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 1ST SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69003
SUBJECT NOMENCLATURE: MICROELECTRONICS

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
4	-	-	4	-	-	30	70	-	-	100

Pre-Requisite: Knowledge of basic BJT

Course Outcomes:

CO1: Review of quantum mechanics.
CO2: To Learn Band theory of solids, bonding forces in solids.
CO3: Discuss Lifetime and recombination theory.
CO4: Review of P-N junction theory.
CO5: Deals with Bipolar transistors– Eber moll & small signal models.

Course Content:

Theory:

UNIT-I
Review of quantum mechanics, Probability and the uncertainty principles, Schrodinger wave equation.

UNIT-II
Motion of electron in a periodic lattice, Band theory of solids, bonding forces in solids, Energy band variation with composition, Effective masses. Fermi levels.

UNIT-III
Statistics of carriers in semiconductors, Lifetime and recombination theory, Boltzmann transport equation, Carrier transport in semiconductor including high field effect.

UNIT-IV
P-N junction theory, Excess currents and break down in p-n junctions. Current flow at junctions. Excess currents and breakdown in p-n junctions.

UNIT-V
Bipolar transistors: Eber moll & small signal models, switching characteristics, Non-uniformly doped transistors, High current and high frequency effects.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. S.M. Sze, Physics of semiconductor devices, Wiley Eastern.
2. B.G. Streetman, Solid State Electronics Devices, PHI.
3. F.Y. Wang, Introduction to solid state electronics, North Holland.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 1ST SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69004
SUBJECT NOMENCLATURE: VLSI TECHNOLOGY

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
4	-	-	4	-	-	30	70	-	-	100

Pre-Requisite: Knowledge of basic Semiconductors

Course Outcomes:

CO1: Understands the basic theory of MOS Transistors, basic steps of fabrication. Learn the basic theory of Crystal growth and preparation.
CO2: Understands the uses of formation and process of silicon dioxide growth, all important Tube furnaces. To learn different types oxidation such as Chemical vapor Deposition, and LPCVD of poly silicon. Oxidation, Kinetics of oxidation.
CO3: Understands the series of processes that establishes the shapes, dimensions and placement of required physical components of IC on the wafer surface layer, understands different types lithography.
CO4: To learn formation of specific "Pockets" of conductive region and N-P in and on the wafer surface, understands the principles and practice of the two doping techniques, diffusion and ion implantation.
CO5: Understands the effect of contaminations on device processing, device performance.

Course Content:

Theory:

UNIT-I
Crystal Growth and Wafer preparation: Wafer terminology, Different crystalline orientations, CZ method, CMOS IC Design flow, Crystal Defects. Fabrication processes of FETs, MOSFETs, and BIMOS etc.

UNIT-II
Layering: Epitaxial growth methods; Technological procedures, modeling redistribution of impurities during epitaxy, evaluation of Epitaxial layers, Chemical vapor Deposition, and LPCVD of poly silicon. Oxidation; Kinetics of oxidation, Deal-Grove model and refinements of this model, impurity redistribution during oxidation, ellipsometry. Metallization; Physical Vapor Deposition, Sputtering, Multi-layer inter connects.

UNIT-III
Patterning: Lithography; Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography. Photo masking steps, Resists, wet and dry etching.

UNIT-IV

Doping: Diffusion; Impurity diffusion; solution of diffusion equation, anomalous diffusion and emitter push effect, modeling of diffusion phenomena, Technological processes for diffusion, Characterization of diffused layers, process simulation of Ion Implantation; Implantation Equipment, Principles, techniques and applications, removal of implant damage.

UNIT-V

Clean room and safety requirements: Types of clean room, Air Filters, HEPA, ULPA, Clean Air strategy, Contamination source, Total clean room strategy, Micro & Mini Environment, Clean Room Construction and Clean room Layout, wafer cleaning.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. S.K.Gandhi, VLSI Fabrication principles, Wiley.
2. S.M. Sze, VLSI Technology, II edition, McGraw Hill.
3. W.R. Runyan, Silicon Semiconductor Technology, McGraw Hill.

References:

1. Y.Chen CMOS Devices and Technology for VLSI, Prentice-Hall.
2. P.VanZant, Microchip Fabrication, A Practical Guide to Semiconductor Processing, Third Edition, McGraw Hill

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 1ST SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69005
SUBJECT NOMENCLATURE: SEMICONDUCTOR DEVICE AND PROCESS MODELLING

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
4	-	-	4	-	-	30	70	-	-	100

Pre-Requisite: Knowledge of basic Semiconductor

Course Outcomes:

CO1: Semiconductor theory is to analyze carrier density and carrier transport an ability to and utilize the basics equations to analyze semiconductor devices.
CO2: To demonstrate an understanding of semiconductor physics and the operation of the most common semiconductor devices at describe the factors that influences the presence of charge carriers in a semiconductor.
CO3: Acquire acknowledgement about basics of memory chip design and technology.
CO4: Introduction of process simulation.
CO5: Identify, formulates and solving problems using the techniques and modern programming tools.

Course Content:

Theory:

UNIT-I
Review of semiconductor theory: Poisson's equation, continuity equation, diffusion equation\drift, current flow equation, finite difference formulation of these equations in 1D and 2D.

UNIT-II
Computation of steady state device characteristic: characteristics of PN junction diode with ideal diode model and real diode model including analysis injection effect. Steady state characteristics of BJT with Eber's moll model and Gummel poon model. Steady characteristics of MOSFET with charge control model, charge sharing model and channel length modulation, MOS capacitor, small signal steady state analysis and transient analysis. Single electron transistor (SET modelling).

UNIT-III

Numerical and computational error, computer memory: SRAM, SDRAM, DDR RAM and CPU, Time requirements, efficient linear solvers, Behavior of Devices, Performance of Devices Circuit simulator: SPICE case study: MINIMOS: Basic features of MINIMOS, MINIMOS6.1, MINIMOS 6.1 WIN, and MINIMOS NT.

UNIT-IV

Process Simulation /Process Modeling: Introduction of process simulation, modeling and simulation of oxidation and diffusion, Ion implantation, Masking, Fick's laws, Case Study: SUPERM.

UNIT-V

Prerequisite: Familiarity with operation of basic semiconductor devices, Knowledge of one programming language, behavior of devices, performance of devices, circuit simulator SPICE.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Seleberherr, Analysis and Simulation of Semiconductor Devices, Springer Verlag.
2. W.L. Engl. Ed. Process and Device Modeling North Holland 1986.
3. R. Raghuram, Computer Simulation of Electronic Circuits, John Wiley.

References Books:

1. K. Lee, M. Shur, T.A. Fjedly & T. Yetterdal, Semiconductor Device Modeling for VLSI, Prentice-Hall.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 1ST SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69201
SUBJECT NOMENCLATURE: APPLICATION SPECIFIC INTEGRATED CIRCUITS (ELECTIVE-I)

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
4	-	-	4	-	-	30	70	-	-	100

Pre-Requisite: Knowledge of basic ASICS

Course Outcomes:

CO1: To focus on different type of ASIC designs with their features which use a library of predesigned and pre -characterized logic cells.
CO2: To discuss on cells, nets and ports, ASIC design software and low level design entry with hierarchy.

Course Content:

Theory:

UNIT-I
Introduction to ASICs: Types of ASICs, Design Flow, Economics of ASICs, ASIC Cell Libraries, ASIC Library Design: Transistors as Resistors, Transistor Parasitic Capacitance, Logical Effort, Library-Cell Design, Library Architecture, Gate-Array Design, Standard-Cell Design, Data path-Cell Design, Programmable ASICs: The Antifuse, Static RAM, EPROM and EEPROM Technology, Practical Issues, Specifications, PREP Benchmarks, FPGA Economics, Programmable ASIC Logic Cells: Actel ACT, Xilinx LCA, Altera FLEX, Altera MA.

UNIT-II
Programmable ASIC I/O Cells: DC Output, AC Output, DC Input, AC Input, Clock Input,Power Input, Xilinx I/O Block, Other I/O Cells, Programmable ASIC Interconnect: Actel ACT, Xilinx LCA, Xilinx EPLD, Altera MAX 5000 and 7000, Altera MAX 9000, Altera FLEX, Programmable ASIC Design Software: Design Systems, Logic Synthesis, The Halfgate ASIC, Low-Level Design Entry: Schematic Entry, Low-Level Design Languages, PLA Tools, EDIF, CFI Design Representation.

UNIT-III
VHDL: A Counter, A 4-bit Multiplier, Syntax and Semantics of VHDL, Identifiers and Literals, Entities and Architectures, Packages and Libraries, Interface Declarations, Type Declarations, Other Declarations, Sequential Statements, Operators, Arithmetic, Concurrent Statements, Execution, Configurations and Specifications, An Engine Controller, Verilog HDL: A Counter, Basics of the Verilog Language, Operators, Hierarchy, Procedures and Assignments, Timing Controls and Delay, Tasks and Functions, Control Statements, Logic-Gate Modelling, Modelling Delay, Altering Parameters, A Viterbi Decoder, Other Verilog Features.

UNIT-IV

Logic Synthesis: A Logic-Synthesis Example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of the Viterbi Decoder, Verilog and Logic Synthesis, VHDL and Logic Synthesis, Finite-State Machine Synthesis, Memory Synthesis, The Multiplier, The Engine Controller, Performance-Driven Synthesis, Optimization of the Viterbi Decoder, Simulation: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation.

UNIT-V

Test: The Importance of Test, Boundary-Scan Test, Faults, Fault Simulation, Automatic Test-Pattern Generation, Scan Test, Built-in Self-test, A Simple Test Example, The Viterbi Decoder Example, Floor planning and Placement: Floor planning, Placement, Physical Design Flow, Information Formats, Routing: Global Routing, Detailed Routing, Special Routing, Circuit Extraction and DRC.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Application-Specific Integrated Circuits, Michael John Sebastian Smith, Addison-Wesley Publishing Company, VLSI Design Series

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 1ST SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69202
SUBJECT NOMENCLATURE: HIGH POWER SEMICONDUCTOR DEVICES (ELECTIVE-I)

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
4	-	-	4	-	-	CW	END SEM	SW	END SEM	
						30	70	-	-	100

Pre-Requisite: Knowledge of basic Power devices

Course Outcomes:

CO1: Understands different types Power Devices.
CO2: Discuss PIN Rectifier in brief.
CO3: Review of different characteristics for power devices.

Course Content:

Theory:

UNIT-I

Introduction: Ideal and typical Power switching waveforms, Ideal and typical Power Device characteristics, Unipolar Power devices, Bipolar Power Devices, MOS-Bipolar Power Devices, Ideal Drift region for unipolar Power Devices, charge- coupled structures: ideal specific On-resistance, Material properties and transport physicsSpace charge generation Lifetime, Recombination Level Optimization, Lifetime Control, Auger Recombination, Ohmic contacts.

UNIT-II

Breakdown voltage: Avalanche breakdown, Abrupt One-dimensional Diode, Ideal specific On-Resistance, abrupt Punch- through Diode, Linearly graded Junction diode, Edge terminations. Schottky Rectifiers: Power Schottky Rectifiers structure, Metal semiconductor contract, forward conduction, reverse blocking, device capacitance, thermal considerations, fundamental tradeoff analysis. P-i-N rectifiers: One-dimensional structure, silicon carbide P-i-N Rectifiers, reverse blocking, switching performance, forward recovery, reverse recovery, P-i-N rectifiers structure with buffer layer, nonpunch-Through P-i-N rectifier structure, P-i-N rectifiers tradeoff Curves.

UNIT-III

Power MOSFETs: Ideal Specific On-resistance, Device Cell structure and operation, Impact of Gate shape, Impact of Cell surface topology, Forward Conduction characteristics, Power VD MOSFET On-Resistance, Power VD MOSFET Cell Optimization, Power U MOSFET On-Resistance, Power U MOSFET Cell Optimization, Square –Law Transfer Characteristics, Super linear Transfer Characteristics, Output Characteristics, Device Capacitances, Optimization for High Frequency Operation, Switching characteristics, Safe Operating Area, Integral Body Diode, High-Temperature characteristics, Complementary Devices,

UNIT-IV

Insulated Gate Bipolar Transistor: Basic Device Structures, Device operation and output characteristics, Device equivalent circuit, Blocking characteristics, On-state characteristics, Current Saturation Model, Switching characteristics, Power loss optimization. Latch-Up Suppression, Deep P^+ Diffusion, Shallow P^+ Layer, Reduced Gate oxide Thickness, Bipolar Current Bypass, Diverter Structure, Cell Topology, Latch-Up Proof Structure Safe operating Area, Forward- Biased Safe Operating Area, Backward- Biased Safe Operating Area, Short-Circuit Safe Operating Area.

UNIT-V

Blocking Voltage Scaling, N-Base Design, Power MOSFET Baseline, On-resistance characteristics, Tradeoff Curve, High Temperature operation, On-state characteristics, Latch up characteristics, Lifetime control technique, Electron irradiation, Neutron irradiation, Helium irradiation, Cell optimization, planner gate structure, Trench-gate structure, reverse conducting structure.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/quizzes and two mid Semester Tests Exam with weightage of 30% of total marks .End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Fundamentals of Power Semiconductor Devices, B. Jayant Baliga
2. Power Electronics and Variable Frequency Drives: Technology and Applications, Bimal K. Bose
3. Modern Power Electronics and Ac Drives Paperback, Bose Bimal K.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 1ST SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69203
SUBJECT NOMENCLATURE: SYSTEM HARDWARE DESIGN (ELECTIVE-I)

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
4	-	-	4	-	-	30	70	-	-	100

Pre-Requisite: Knowledge of basic Digital Electronics, CMOS Design

Course Outcomes:

CO1: Review of Sequential and Combinational circuits.
CO2: Deals with Power distribution, clocking strategy.
CO3: Design Synchronous and Asynchronous design and multilayer PCB design
CO4: Optimization Noise tolerant design.
CO5: Study of different types memory based subsystems.

Course Content:

Theory:

UNIT-I
Advance digital logic design: Sequential, Combinational and State Machines, Design issues based on power dissipation, timing and loading and case studies , CMOS , BICMOS and TTL noise and ESD issues.

UNIT-II
Basic System Design aspect: Power distribution, Clocking strategies, Clocked system, Latch and Resistors, System timing, two phase clocking, four phase clocking, Clock distributions, Signal connection and Signal quality.

UNIT-III
Synchronous and Asynchronous design and multilayer PCB design. Interface between devices, boards and units

UNIT-IV
Transient switching problems and worst case timing. Timing analysis and optimization Noise tolerant design, EMI related design aspects, Noise in MOS transistors and resistors, Noise examples.

UNIT-V
Memory based subsystem design, Static RAM, Dynamic Ram, Field programmable gate array (FPGA), CPLD based design. Microcontroller (8 bit and 16 bit) and their applications, Analog design issues some examples of real life system.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Modern VLSI Design: System on chip design by wayne wolf (Pearson Education).
2. VLSI Design techniques for Analog and Digital Circuits, Randall L. Geiger, Philip E. Allen, Noel R Strades, McGraw Hills Publications.
3. Analog Integrated Circuit Design by David Johns, Ken Martin, John Wiley publications.

References Books:

1. CMOS Analog Circuit Design by Philip E Allen, Douglas R Holberg, Oxford publications.
2. FPGA Based Design, Wolf, Pearson Education

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 1ST SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69204
SUBJECT NOMENCLATURE: HARDWARE DESCRIPTION LANGUAGES (ELECTIVE-1)

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
4	-	-	4	-	-	30	70	-	-	100

Pre-Requisite: Knowledge of basic logic gates, Digital Electronics

Course Outcomes:

CO1: Discuss different types design styles such as Structural, Data-flow and Behavioral styles.
CO2: In this subject understand Variable and signal types, arrays and attributes.
CO3: Use of Procedures and functions.
CO4: Discuss Verilog module.
CO5: Understand Task and Function.

Course Content:

Theory:

UNIT-I: Basic concepts of hardware description languages, Hierarchy, Concurrency, Logic and Delay modeling, Structural, Data-flow and Behavioral styles of hardware description. Architecture of event driven simulators

UNIT-II: Syntax and Semantics of VHDL, Variable and signal types, arrays and attributes. Operators, expressions and signal assignments. Entities, architecture specification and configurations, Component instantiation.

UNIT-III: Concurrent and sequential constructs. Use of Procedures and functions, Examples of design using VHDL

UNIT-IV: Syntax and Semantics of Verilog. Variable types, arrays and tables. Operators, expressions and signal assignments. Modules, nets and registers

UNIT-V: Concurrent and sequential constructs. Tasks and functions, Examples of design using Verilog. Synthesis of logic from hardware description.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1 J. Bhaskar, "VHDL Primer", Pearson Education Asia 2001.
2 Z. Navabi, "VHDL", McGraw Hill International Ed. 1998.
3 S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall NJ, USA), 1996.

References Books:

1. J. Bhaskar, "Verilog HDL Synthesis - A Practical Primer", Star Galaxy Publishing, (Allentown, PA) 1998.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 2nd SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69501
SUBJECT NOMENCLATURE: COMMUNICATION RF IC DESIGN

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
4	-	-	4	-	-	CW	END SEM	SW	END SEM	
						30	70	-	-	100

Pre-Requisite: Knowledge of RF Communication

Course Outcomes:

CO1: Recall RF & transmission line theory
CO2: Understand the design bottleneck specific to RFIC design, linearity related issues, ISI.
CO3: Identify noise sourses & develop noise models for MOS devices & circuits.
CO4: Specify noise & interference performance matrices like noise figure, 11P3, Gain & matching.
CO5: Construct RF receiver front end with various blocks & topologies.
CO6: Design various constituents blocks of RF receiver front end.

Course Content:

Theory:

UNIT-I
Review of RF Theory: RF range, skin effect, behavior of various passive components like R, L, C, at high RF, their equivalent circuits at high RF. Transmission line theory, reflection coefficient, Smith chart calculation, impedance matching, S-parameter.

UNIT-II
Basic concepts in RF design: RF dc design. Hexagon wireless communication standards, non-linearity, harmonics, gain compression, desensitization, cross modulation, inter modulation distortion (IMD), input intercept point (IIP3 & IIP2), inter symbol interference. Noise, types of noise, noise analysis of active devices.

UNIT-III
Trans-receiver Architecture: TRF receivers, heterodyne receivers, Homodyne receivers, their comparison, type RF receiver architecture and its design.

UNIT-IV
Design concepts-1: Low noise amplifiers, various topologies, comparison and design. Mixers, various topologies, comparison and design. Filters- type and design.

UNIT-V

Design Concepts-2: Oscillator, various types comparison and design. Frequency synthesizes and their design IC application and case studies for DECT, GSM and Bluetooth.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. RF Microelectronics- BehzadRazavi, PHI.1998.
2. RF circuit design- R. Ludwig and P. Bretcheko PHI.2000.
3. The design of CMOS radio frequency integrated circuits by Thomas H. Lee. (Cambridge university press.1998)

References Books:

1. RF and Microwave circuit design for wireless communication. L.E Larson (Arteech House Publication 1997)

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 2nd SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69502
SUBJECT NOMENCLATURE: MIXED SIGNAL CIRCUIT DESIGN

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
4	-	-	4	-	-	CW	END SEM	SW	END SEM	
						30	70	-	-	100

Pre-Requisite: Knowledge of basic Analog and Digital circuits

Course Outcomes:

CO1: Present scenario presence mixed signal circuits because commercial and industrial application based on same.
CO2: In communication systems and digital processing mixed circuit being used.
CO3: Now days VLSI, based on Mixed signal circuits.
CO4: In RF IC design mixed signal circuit in highly appreciable.
CO5: Software for CAD in VLSI based on mixed signal circuits deign.

Course Content:

Theory:

UNIT-I
BiCMOS devices and technology: BiCMOS inverter and logic gates, Characteristics, Noise Margin and Power dissipation, BiCMOS operational Amplifier, Comparison of BiCMOS, Bipolar and CMOS technology.

UNIT-II
Basic Analog and Digital sub circuit: Switches, Active resistors, Current sinks and sources, Current mirrors, current and voltage references, Band gap reference, Power dissipation and noise analysis.

UNIT-III
Current mode signal processing: Current conveyor, current mode differentiator, Integrator, summer. Advantage of current mode circuits. Current normalizer, current correlator and Bump circuit.

UNIT-IV
Continuous time and sampled data signal processor, Current scaling D/A, voltage scaling, charge scaling D/A, Nyquist rate ADC, Pipe line ADC, Interpolating ADC, Folding ADC, Over Sampled ADC, Delta Sigma ADC, ADC & DAC characteristics and parameters.

UNIT-V
Analog VLSI Interconnects: Physics and Scaling of interconnects logic and interconnect design, delay modeling, wire sizing, buffer insertion, cross talk minimization, resistive, capacitive and inductive interconnects.

UNIT-VI Statistical modeling of devices and circuits: Computer Aided analog design, CAD system, T-SPICE, Analog and Mixed (Analog and digital) circuit layouts.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. VLSI Design techniques for Analog and Digital Circuits, Randall L. Geiger, Philip E. Allen, Noel R Strades, McGraw Hills Publications.
2. Analog Integrated Circuit Design by David Johns, Ken Martin, John Wiley Publications.
3. CMOS Analog Circuit Design by Philip E Allen, Douglas R Holberg, Oxford publications.

References Books:

1. CMOS Circuit Design Layout and Simulation by Jacob Baker, Harry W.Li, David E. Boyce, PHI.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 2nd SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODEEI 69503
SUBJECT NOMENCLATURE: VLSI TEST AND TESTABILITY

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
4	-	-	4	-	-	CW	END SEM	SW	END SEM	
						30	70	-	-	100

Pre-Requisite: Knowledge of Testing

Course Outcomes:

CO1: This gives knowledge about testing process at IC level with their functions and relations.
CO2: Introduces the major concepts of all test techniques such as redundancy, fault coverage, sensitization and backtracking.
CO3: It discusses test generation for combinational and sequential circuits both it examines in detail
various techniques available for fault detection.
CO4: Deals with test generation and response evaluation techniques used in built-in-self-test (BIST) Schemes for VLSI chips some popular BIST architectures are examined.
CO5: It discusses the fundamental of fault detection and also introduces the concept of controllability, observably and fault equivalency.

Course Content:

Theory:

UNIT-I
Fabrication Assembly and Test Process: Introduction to testing process, types of testing at IC level, IC production test process, Burn-in-Board, system and field testing, cost of testing. Relations and functions, Boolean function representation canonicity and equivalence Boolean satisfiability.

UNIT-II
Fault Modeling and Simulation: Circuit modeling, Introduction to fault, fault detection and redundancy, fault equivalence and fault dominance, Stuck at fault, bridging faults, transistor faults, delay faults etc. fault collapsing and fault sampling simulation, simulation techniques, compiled simulation, event-driven simulation, series, parallel deductive and concurrent fault simulation.

UNIT-III
Test generation for combination and sequential circuits: D-algorithm, PODEM, Boolean satisfiability, automatic test pattern generation, primitive and propagation cubes, path oriented decision making, fan-out oriented test generation, DFT for combinational and sequential digital circuits. LSSD techniques

UNIT-IV

Built in self-test and IDDQ testing: RAM BIST, logic BIST, BIST pattern generation and response analyzer, scan based BITS architecture, random and weighted random pattern testability, test point insertion for improving random testability. Fundamental of IDDQ testability. Case studies.

UNIT-V

Design for testability: Controllability & observability, Models of sequential circuits, state table method, self-initializing test sequences, undetectability, distinguishing and synchronizing sequences, and complexity of sequential ATGP. Built in self-test for VLSI chips

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Parag K lala, Self-checking and fault tolerance Digital Design , Academic press.
2. P.K. lala Digital Circuit Testing and Testability, Academic press.
3. Alfred L Crouch , Design for Test ,PTR PH

References Books:

1. M. Abramovici, M.A. Brever, A.D. friedman , Digital system testing and testable Design, IEEE Press.
2. Chakraborty, Fault Tolerance and reliability, Pearson education.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 2nd SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EE 69505
SUBJECT NOMENCLATURE: DIGITAL SIGNAL PROCESSING

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
4	-	-	4	-	-	CW	END SEM	SW	END SEM	
						30	70	-	-	100

Pre-Requisite: Knowledge of basic communication

Course Outcomes:

CO1: Learn characteristics of signals & systems like time invariant, linear nonlinear, causal etc.
CO2: Gain knowledge of Z-transform & analyzing discrete system using Z-transform.
CO3: Designing digital filters & their implementation.

Course Content:

Theory:

UNIT-I
Discrete time signals: Sequences & systems, linear time invariant systems & their properties. Difference equations. Frequency domain representations of discrete time signals & systems. Discrete time Fourier transform of (DTFT).

UNIT-II
Sampling of continuous time signals., Freq. domain representation of sampling, reconstruction of a band-limited signal from its samples, discrete time processing of continuous time signals, continuous time processing of discrete time signals, changing the sampling rate using discrete time processing.

UNIT-III
Z-transform – properties of Z-transform, properties of the region of coverage for the Z-transform, inverse Z-transform using contour integration, complex convolution theorem, parseval's relation, unilateral Z-transform. Transform analysis of linear time invariant systems- - Frequency response of LTIV systems, systems functions frequency response for rational system functions, relationship between magnitude & 1-phase, All-pass systems, Minimum phase system.

UNIT-IV
Structures of discrete time systems: Signal flow graph representation of linear constant coefficient difference eqn. Basic structures of FIR & IIR systems. Design of FIR filters by windowing, Kaiser Window. Design of IIR filters from contentious time filter.

UNIT-V
Discrete Fourier Transform (DFT) & its properties, linear convolution using DFT decimation in time FFT algorithm, implementation of the DFT using convolution. Discrete Hilbert transformer.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Discrete-Time Signal Processing – Alan V. Oppenheim & Ronald W. Schafer, PHI, Pvt., Ltd., New Delhi, 1997.
2. Theory and Application of Digital Signal Processing – L. R. Rabiner& B. Gold, Prentice-Hall Englewood Cliffs, NJ 1975.
3. Digital Signal Processing, Proakis, PHI.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 2nd SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69701
SUBJECT NOMENCLATURE: IMAGE PROCESSING (ELECTIVE-II)

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
4	-	-	4	-	-	CW	END SEM	SW	END SEM	
						30	70	-	-	100

Pre-Requisite: Knowledge of basic DSP

Course Outcomes:

CO1: Discus Digital Image Fundamentals.
CO2: Review of Image Enhancement in the Frequency Domain.
CO3: Deals with Image Restoration.
CO4: understands Image Segmentation, Representation and Object recognition.

Course Content:

Theory:

UNIT-I Digital Image Fundamentals.

Elements of Visual Perception. Image Sensing, Acquisition, Sampling and Quantization. Some Basic Relationships between Pixels. Linear and Nonlinear Operations. Gray Level Transformations. Histogram Processing. Enhancement Using Arithmetic/Logic Operations. Basics of Spatial Filtering. Smoothing Spatial Filters. Sharpening Spatial Filters. Combining Spatial Enhancement Methods.

UNIT-II Image Enhancement in the Frequency Domain.

Background. Introduction to the FourierTransform and the Frequency Domain. Smoothing, Frequency-Domain Filters. Sharpening Frequency Domain Filters. Homomorphic Filtering. Implementation.

UNIT-III Image Restoration.

A Model of the Image Degradation/Restoration Process. Noise Models. Restoration in the Presence of Noise Only-Spatial Filtering. Periodic Noise Reduction by Frequency Domain Filtering. Linear, Position-Invariant Degradations. Estimating the Degradation Function. Inverse Filtering. Minimum Mean Square Error (Wiener) Filtering. Constrained Least Squares Filtering. Geometric Mean Filter. Geometric Transformations.

UNIT-IV Image Segmentation, Representation and Object recognition

Detection of Discontinuities. Edge Linking and Boundary Detection. Thresholding. Region-Based Segmentation. Segmentation by Morphological Watersheds. The Use of Motion in Segmentation.Representation. Boundary Descriptors. Regional Descriptors. Use of Principal

Components for Description. Relational Descriptors. Patterns and Pattern Classes. Recognition Based on Decision-Theoretic Methods. Structural Methods. Color Fundamentals. Color Models. Pseudocolor Image Processing. Color Transformations. Smoothing and Sharpening. Color Segmentation.

UNIT-V Fundamentals. Image Compression Models. Elements of Information Theory. Error-Free Compression. Lossy Compression. Image Compression Standards. Multi-resolution Expansions. Wavelet Transforms in One Dimension. The Fast Wavelet Transform. Wavelet Transforms in Two Dimensions. Wavelet Packets. Computer Vision.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Rafael C Gonzalez, Richard E Woods 2nd Edition, Digital image Processing Pearson Ed.

References Books:

1. William K Pratt, Digital Image Processing John Willey(2001)
2. Image Processing Analysis and Machine Vision-Milman Sonka, Vaclav hiavac, Rogar B.
3. A.K. Jain, PHI, NewDelhi (1995)-Fundamentals of Digital Image Processing.
4. Chanda Dutta Magundar-Digital Image Processing and Applications, Prentice Hall of In.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 2nd SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69702
SUBJECT NOMENCLATURE: MICROWAVE INTEGRATED CIRCUITS (ELECTIVE-II)

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
4	-	-	4	-	-	CW	END SEM	SW	END SEM	
						30	70	-	-	100

Pre-Requisite: Knowledge of basic Microwave engineering

Course Outcomes:

CO1: Description of a series of novel passive elements and devices introducing terminations and planer inductors, miniature directional couplers divider etc.
CO2: To discuss on principle concepts of design and fabrication technology.it gives knowledge on different packaging techniques.

Course Content:

Theory:

UNIT-I
Introduction, characteristics of Planner Transmission Lines, Strip Line, Analysis of Microstriplines, Variational Methods, Conformal Transformation, Suspended Stripline, Slot Line, Coplanar Waveguide, Fin Line, characteristics of Print Coupled Lines, Microstrip Coupled Lines, Coupled suspended Striplines, Coupled Slotlines and coplanar waveguide, Irregular lines.

UNIT-II
Distributed and Lumped Elements of Integrated Circuits, Capacitor, Inductor, Resistors, Terminators and Attenuators, Resonators, Discontinuities, Common feature and parameters of Networks, Multiport Network as "Pandora's Box", Common features and Parameter of Two port Network, Some advantages of four port network Matrix correlation for coupled Lines, Numerical Analysis, Losses in Microstriplines. Slotted Lines, Coupled Lines,

UNIT-III
Design of Directional Couplers, Hybrid Couplers, Filters, Ring Directional Couplers, Branch-Line Directional Couplers, Coupled-line Directional Couplers, Circulated, Microstriplines with ferrite & Garnet Substrate Lumped Elements in MICs.

UNIT-IV
Dividers and combiners: T- and Y- Junctions, Dividers and Combiners on Directional Coupler base, In-Phase Quarter wavelength Power Dividers/ Combiners, N-Way Dividers/ Combiners, Filters: Classification, Filter synthesis, LPFs, BPFs, Pin Diode parameters, Switches, Classification, Basic configurations, Multiple- Diode Switches, Transmit-Receive Switches,

Attenuators, Reflective Attenuators, Non-reflective Attenuators, Switched Channel Attenuators, Limiters. Phase Shifters, Circulators and Isolators.

UNIT-V

Technology of MICs, Monolithic Hybrid Substrate, Thin & Thick Film Techniques RF/ Microwave packages, Metal Packages, Ceramic packages, plastic packages, Three-Dimensional Design, Horizontal-Vertical Configuration, Multilayer Structures, Fabrication aspects, HMICs, MMICs, Computer Aided Design.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Passive RF & Microwave Integrated circuits, Leo G. Maloratsky, Newnes, Elsevier
2. Modern Communication Circuits by Jack R. Smith, MGH.
3. RF Microelectronics by Behzad Razavi, PHI.

References Books:

1. RF and Microwave Circuit Design for Wireless Communication by L.E. Larson, Artech House Publications.

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 2nd SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69703
SUBJECT NOMENCLATURE: OPTOELECTRONIC INTEGRATED CIRCUITS (ELECTIVE-II)

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
4	-	-	4	-	-	CW	END SEM	SW	END SEM	
						30	70	-	-	100

Pre-Requisite: Knowledge of Optical Communication

Course Outcomes:-

CO1: To discuss waveguides and its types with its advantages and disadvantages.
CO2: To learn waveguide fabrication and characterization
CO3: To discuss optical coupling, switching & optical modulator.
CO4: Illustration of latest development in optoelectronics, lasers and detectors.

Course Content:

Theory:

UNIT-I
Theory of Optical Waveguides: Waveguide theory: one dimensional planar waveguides, two dimension waveguide, transcendental equations, waveguide modes, mode cutoff conditions.

UNIT-II
Optical waveguide fabrication and characterization : waveguide fabrication : Deposited films; vacuum deposition and solution deposition, diffused waveguides, ion exchange and ion implanted waveguides , Epitaxial growth of III-V compound semiconductor materials , shaping of waveguides by wet and dry etching techniques. Waveguide characterization: surface scattering and absorption losses, radiation and bending losses, measurement of waveguides loss, waveguide profiling.

UNIT-III
Fundamental of optical coupling: Transverse coupler, prism coupler, grating coupler, fiber to waveguide coupler, coupling between optical waveguides, directional coupler. Application of directional coupler.

UNIT-IV
Guided wave modulators and switches: Physical effect used in light modulators: electro-optic, acousto-optic, and magneto-optic effects. Waveguide modulators and switches. Semiconductor laser and detectors: laser diode, distributed feedback lasers. Integrated optical detectors.

UNIT-V
Recent progress in integrated optics: state of art technology in guided wave devices and application, e.g. photonic switching,tunable laser diodes, optical integrated circuits.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. T Tamir (Ed), Guided wave optoelectronic, (Springer – Verilog, 1990).
2. R Sysm& J Cozens: Optical guided waves and devices, (McGraw- Hill, 1993).

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
M.TECH 1ST YEAR/ 2nd SEMESTER (MICROELECTRONICS & VLSI DESIGN)
SUBJECT CODE: EI 69704
SUBJECT NOMENCLATURE: LOW POWER VLSI DESIGN (ELECTIVE-II)

PERIOD PER WEEK			CREDITS			MAXIMUM MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
4	-	-	4	-	-	30	70	-	-	100

Pre-Requisite: Knowledge of basic CMOS

Course Outcomes:

CO1: Introduction to low power VLSI design-Need for low power-CMOS leakage current-static.
CO2: Deals with Pre-computation logic.
CO3: Discuss Power reduction in clock networks- CMOS floating node- low power bus-delay balancing- SRAM.
CO4: Understands Algorithm and architectural level methodologies- Introduction, design flow.
CO5: Discuss different type deign style.

Course Content:

Theory:

UNIT- I: Introduction to low power VLSI design-Need for low power-CMOS leakage current-static current-Basic principles of low power design-probabilistic power analysis-random logic signal-probability and frequency-power analysis techniques-signal entropy.

UNIT-II: Circuit- transistor and gate sizing- pin ordering- network reconstructing and reorganization-adjustable threshold voltages-logic-signal gating-logic encoding. Pre-computation logic.

UNIT-III: Power reduction in clock networks- CMOS floating node- low power bus- delay balancing- SRAM. Switching activity reduction, parallel voltage reduction, operator reduction- Adiabatic computation- pass transistor logic.

UNIT-IV: Algorithm and architectural level methodologies- Introduction, design flow, algorithmic level analysis and optimization, architectural level estimation and synthesis.

UNIT-V: Low power circuit design style- Software power estimation –co design.

Assessment:

Continuous evaluation of students through: Class attendance, Assignments, organizing Seminars/Quizzes and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

Text Books:

1. Gary Yeap, Practical Low Power Digital VLSI Design, McGraw hill, 1997.
2. Kaushik Roy, Sharat C. Prasad, Low Power CMOS VLSI circuit design, Wiley Inter Science Publications, 1987.

Reference Books:

1. Rabaey, Pedram, "Low power design methodologies" Kluwer Academics, 1997.
2. Anantha P. Chandrakasan & Robert W. Brodersen, "Low Power Digital CMOS Design" Kluwer Academics Publications, 1994.
3. A. Bellameur & M.J. Elmauri- Low Power VLSI CMOS circuit design, Kluwer Academics Press, 1995.