VLSI Design

ⓐ VHDL Modelling

i) Data flow modelling
ii) Behavioral —11—
iii) Structure —11—
iv) Mixed —11—

In terms of engg. we are interested in the Mathematical modelling.

ⓐ HALF ADDER

The library which we generally use is (IEEE)

the package we use from the library is (std_logic_1164.all)

entity - define i/p & o/p

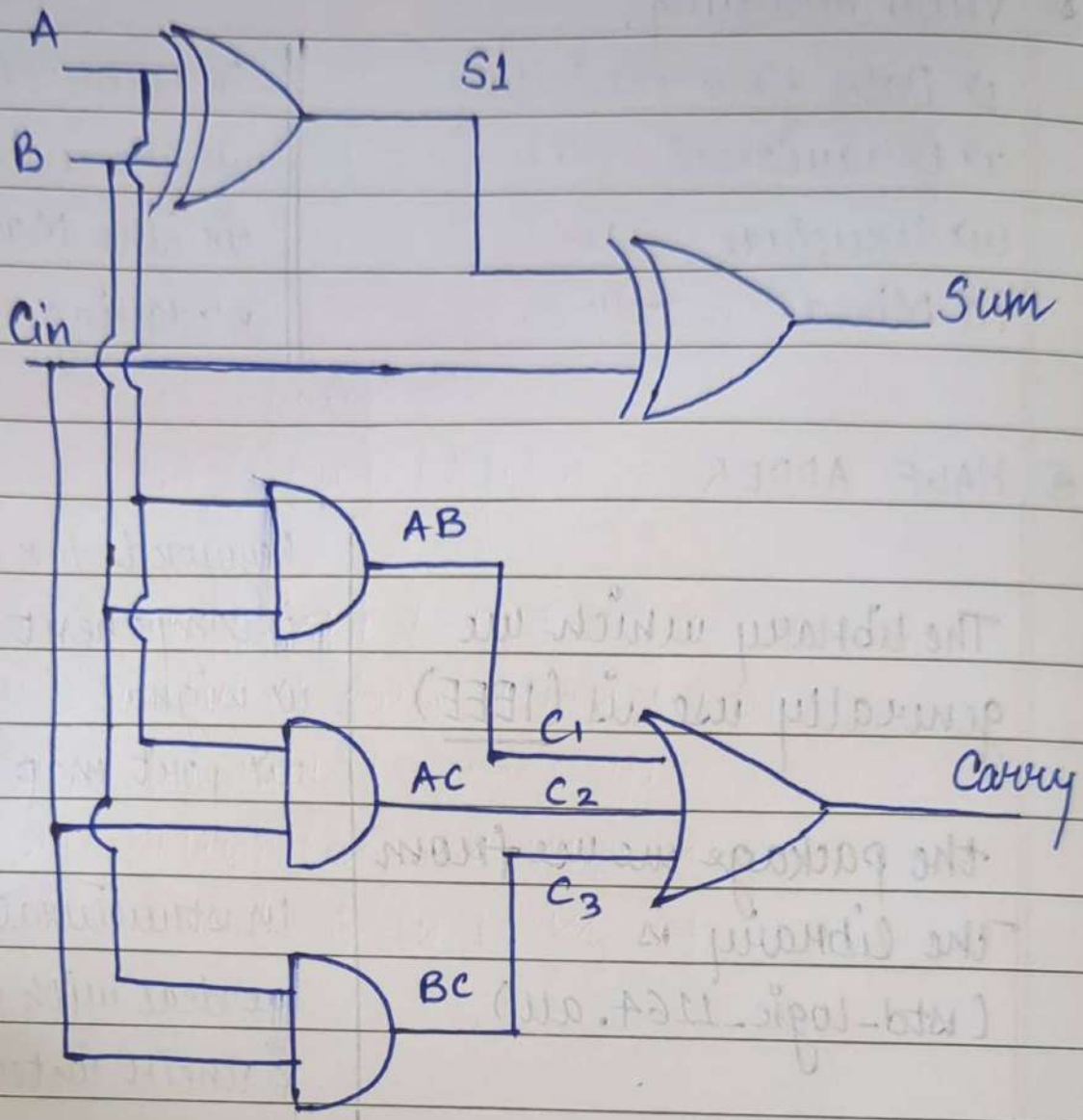
Keywords for structural
i) component
ii) signal
iii) port map

In structural modelling we deal with comp. info & their interconnection

```
Library IEEE library          -- library
use std_logic_1164.all        -- package

Entity                        } entity
  A, B, Cin : IN  std_logic   }
  Sum, Carry : OUT std_logic  }

Architecture
```



⊛ Structural Modelling

For structure modelling, we deal with components & their interconnection:

Component

Component XOR21
    A, B = in _ std_logic
    C = out _ std_logic

```
Component AND21
        A, B : in std_logic
        C : out std_logic

Component OR21
        A, B, C : in std_logic
        D : out std_logic
```

we are not interested in defining all gates, we only define "Types of components"

(we use signal to define intermediate signals)

```
Signal S1, C1, C2, C3 std_logic
U1: XOR21 portmap (A, B, S1)
U2: XOR21 portmap (S1, Cin, Sum)
U3: AND21 portmap (A, B, C1)
U4: AND21 portmap (A, Cin, C2)
U5: AND21 portmap (B, Cin, C3)
U6: OR21 portmap (C1, C2, C3, Carry)
```

before component is the block of code from library IEEE to entity [last page wala]

here we have defined the i/p o/p ports and linked them with intermediatory signals

⭐ VLSI design style

100% custom ↓ 0%

1) Full custom design (each & every transistors are led down by designers)
2) Semi custom design
   - Standard cell based design
   - ↳ GATE array
   - ↳ FPGA / CPLD / PLD's

In Full custom design, we are concerned about W/L ratio of each transistor. Even the type of metal layer/wire which are interconnecting them. They start from scratch. They are best in terms of area, speed, power.

In Semi custom design most of the components are used which are prebuilt (library) & for the rest of components, we can design on our own.

On the basis of their customisation, we can broadly classify them as Fully, semi but for the point of understanding we can also add PLD based. i.e Full, semi & PLD.

Time to market:- best FPGA > Semi > Full
lowest fastest

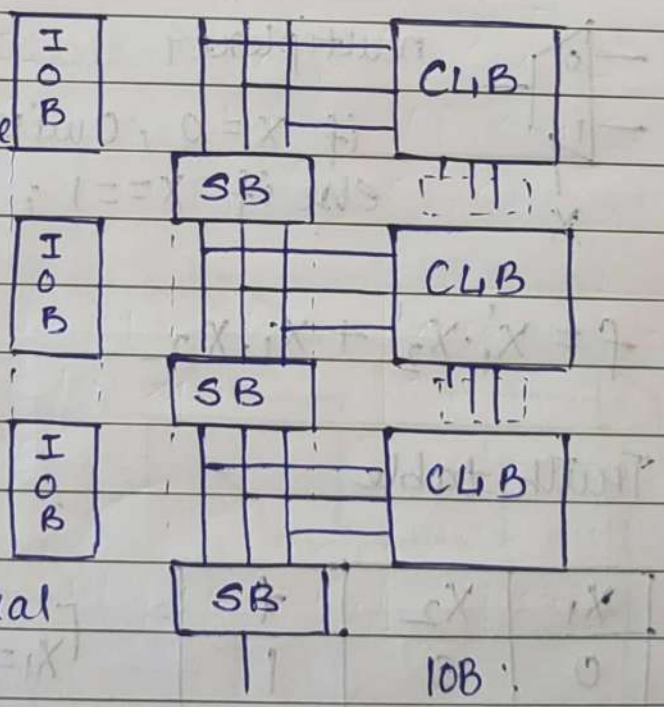
[ASIC : application specific IC]

Parameters:	Full	Semi	FPGA
Time to market	max	< : >	min
cost	max (if fabricating single)	< >	min
performance	best (ASIC) ☺	in b/w	not feasible
area	min	in b/w	max

FPGA

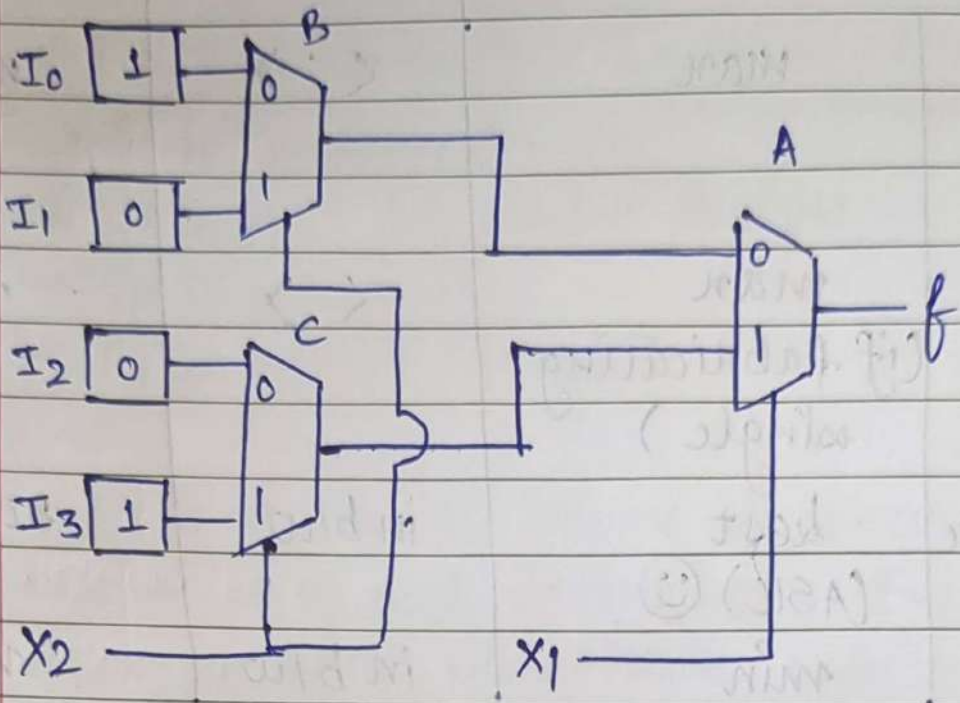
28-09-2022

- Field Programmable Gate Array
  - can be used in field. (General purpose)
- OS & IS. (IC)
  Interconnecting wires can be programmed

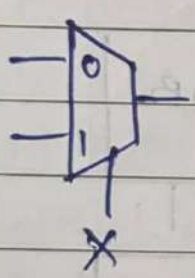


IOB:
- Interconnect [wires]
- Configurable logic blocks
- switch box

⊛ CLB: Configurable logic block



LUT: look up table



multiplexer

if X = 0, 0 will be selected.
else if X == 1; 1 channel will be selected.

$f = X_1' \cdot X_2' + X_1 \cdot X_2$ (2:1 multiplexer)

↳ lookup

Truth table

X_1	X_2	f
0	0	1
0	1	0
1	0	0
1	1	1

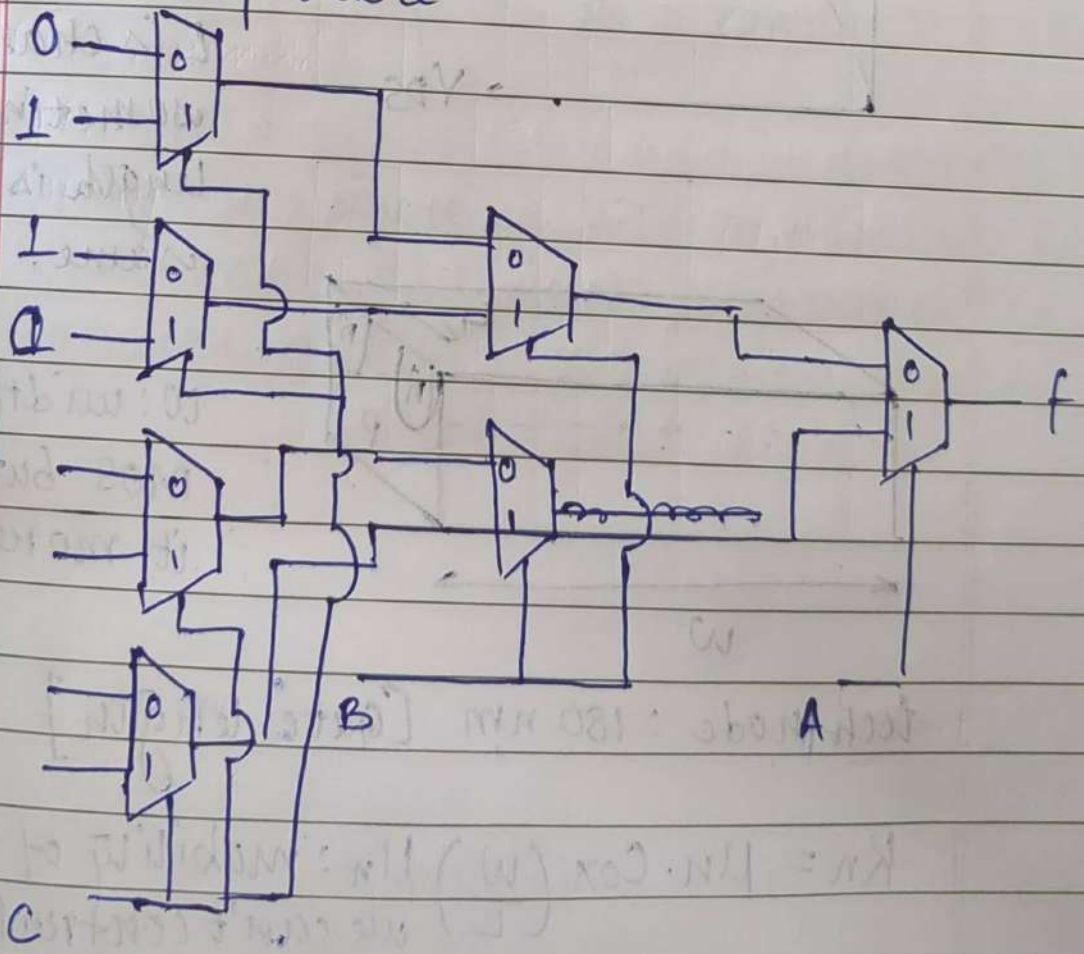
[$X_1 = 0, X_2 = 0$,
A will use ch:0,
B & C will use 0 also
but C's o/p will be
deselected]

Making adder using previous ckt

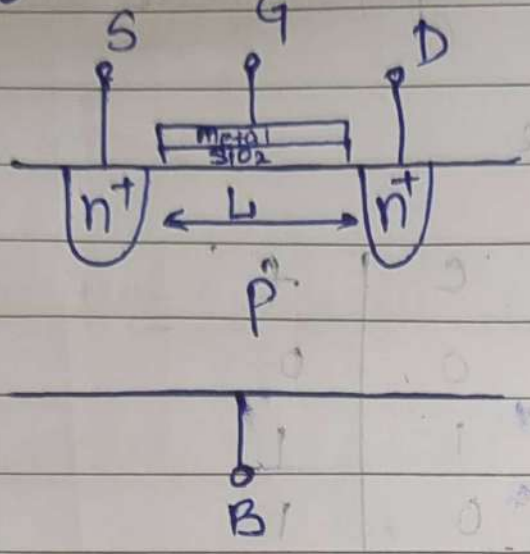
Truth Table

A	B	C	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

look up table



MOS

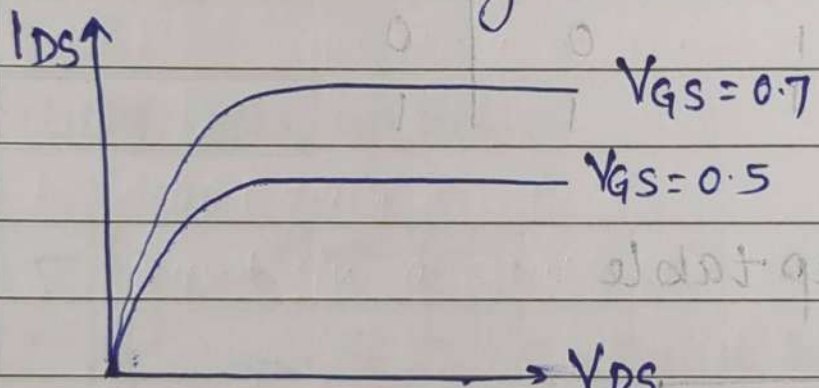


$$I_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right)(V_{gs} - V_t)^2$$

[Nowadays, we use polysilicon as metal level instead of Aluminium. ↓]

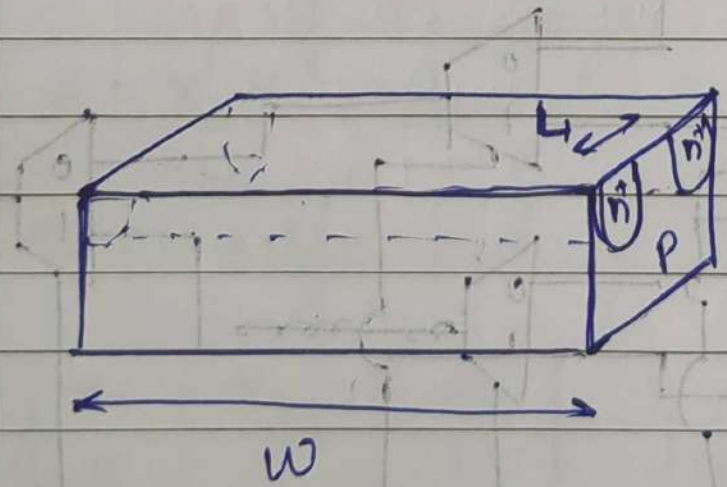
⇒ Characteristics of MOS

- Threshold voltage (V_t)



[the W/L in I_D is design variable.]

L is channel length sometimes gate length is nearly same.



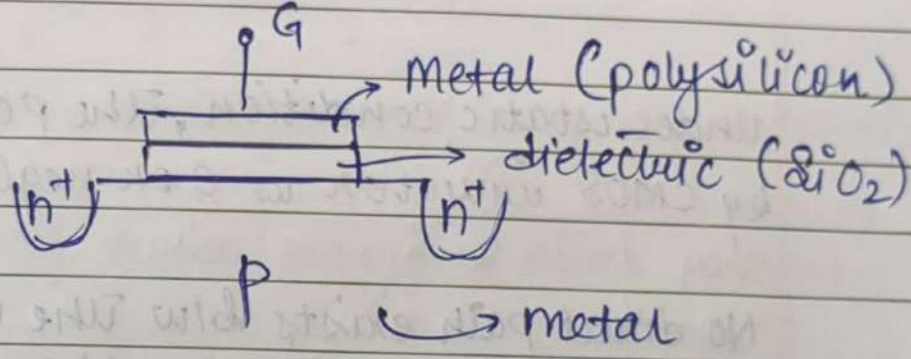
W: width of MOS but we won't it more. ie

tech node : 180 nm [Gate length]

$K_n = \mu_n \cdot C_{ox} \left(\frac{W}{L}\right)$ μ_n : mobility of $e^\ominus$ we can't control

Cox : oxide capacitance = $\frac{\varepsilon_{ox}}{t_{ox}}$

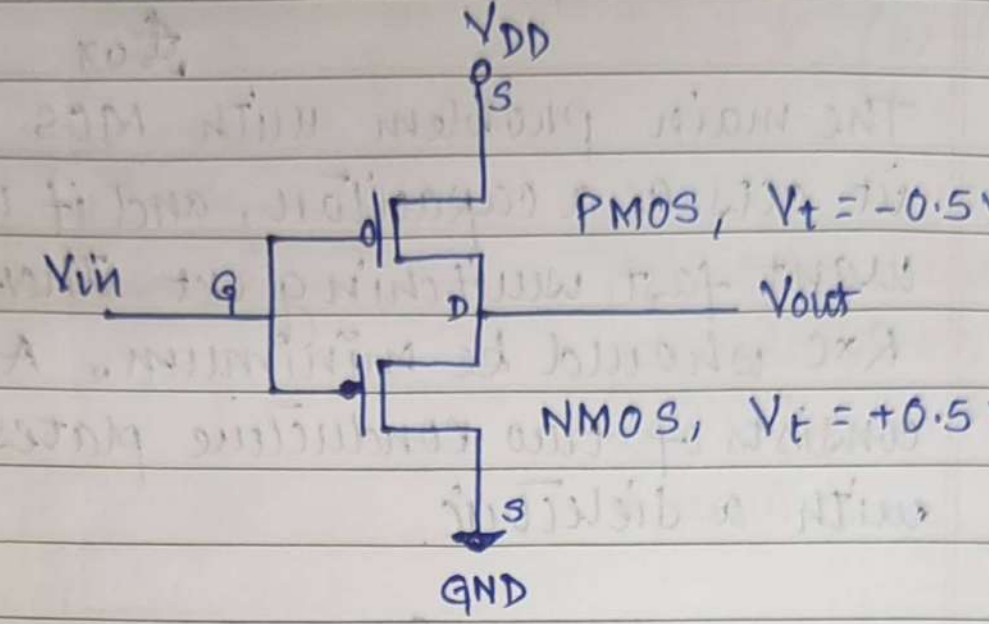
The main problem with MOS is that it acts as a capacitor, and if we want want fast switching ckt then value of R×C should be minimum. Any capacitor consists of two conductive plates filled with a dielectric.



$C = \frac{\varepsilon_0 A}{d}$, here ε_0 is a constt & $A = W \times L$ so we deal with W/L

If we increase W then W/L will be favourable but it will increase the capacitance which is not favourable.

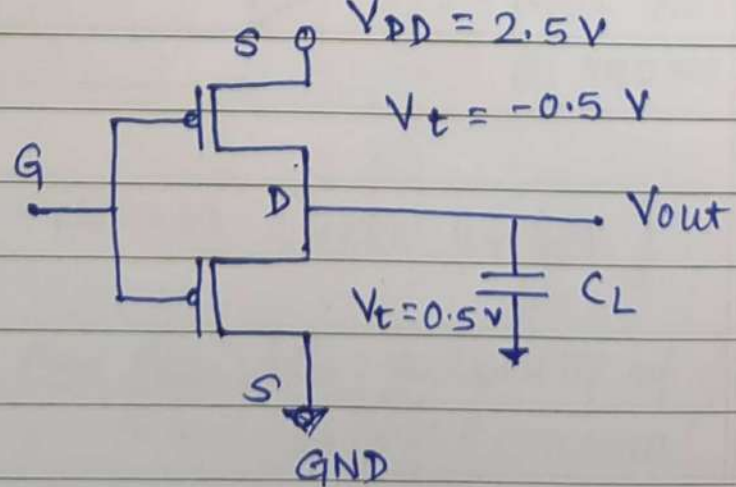
⊛ CMOS Inverter



Under static condition, the power drawn by CMOS inverter is 0 or negligible.

No direct path exists b/w the supply voltage & ground in a static condition.

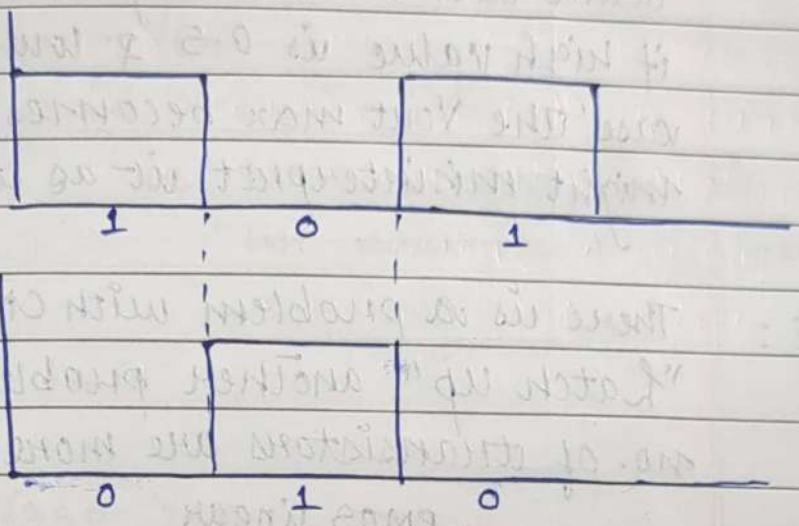
When we have a NMOS, then the threshold is going to be some the value as we need to create a channel. The V_{GS} is used to determine whether the NMOS is in on state or not.
i.e $V_{(GS)n} > V_t$ here V_t is threshold voltage



$$I_D = K_n\left[\left(\frac{W}{L}\right)(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

transfer characteristics

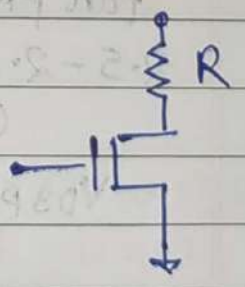
VTC: Voltage ~~transmission~~ curve



the above characteristic is of ideal condition we need to understand the VTC curve as to study noise margin & other params.

Fan-out : how many CMOS units can we connect with the Vout of previous. Ideally we can connect infinite no. of inverters but practically there is some leakage i.

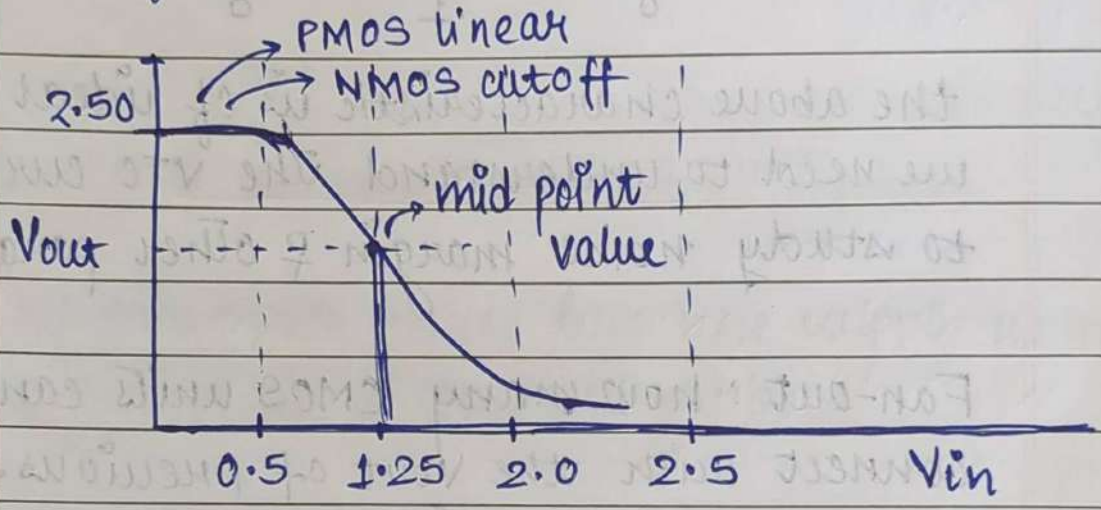
In comparision to the resistor of NMOS, the PMOS is CMOS offers less resistance.



Full swing is the parameter which determines the max achievable output voltage and min -11-.

we need more noise margin, so that the device won't misinterpret the output. ex: if high value is 0.5 & low is 0.0 but in case the Vout max becomes 0.3 the CMOS might misinterpret it as low signal.

NOTE: There is a problem with CMOS known as "Latch up". another problem is that the no. of transistors are more.



$V_{DS} = V_{GS} - V_t$ for $V_{in} = 0.5$

for PMOS

$2.5 - 2.5 = -2.0 - (-0.5)$

$0 = -1.5$

$V_{DSP} > -1.5$ for PMOS

$$\boxed{V_{DSP} \geq V_{GSP} - V_t}$$

it means PMOS is in linear reg

PMOS is complementary to NMOS in all params so saturation of PMOS is

$$\boxed{V_{DSP} \leq V_{GSP} - V_{tp}}$$

Now checking for NMOS at $V_{in} = 0.5$ V

$V_{DSN} = V_{GSN} - V_{tn}$

$2.5 - 0.0 = (0.5 - 0.0) - 0.5$

$V_{DSN} \geq 0$ ie NMOS is operating in the saturation region.

for $V_{in} = 1.25$

PMOS

$V_{DSP} = V_{GSP} - V_{tp}$

$1.25 - 2.5 = (1.25 - 2.5) - (-0.5)$

$-1.25 = (-1) + 0.5$

$-1.25 = -0.5$

$V_{DSP} \geq -0.5$ i.e PMOS is in saturation

NMOS

$1.25 - 0 = (1.25 - 0) - (0.5)$

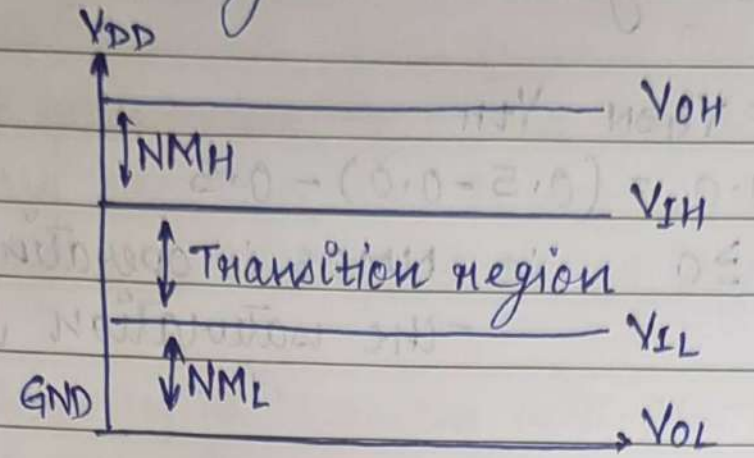
$1.25 = 0.75$ NMOS is in saturation

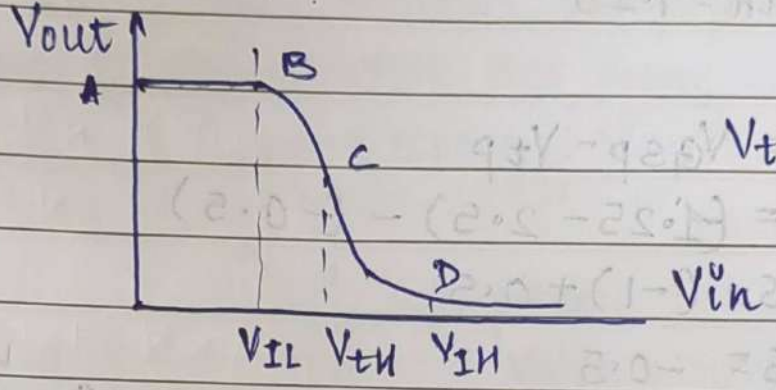
for $V_{in} = 2.0$.

~~$V_{DS} = V_{GS} - V_t$~~ PMOS : saturation

~~$V_t =$~~ NMOS : linear

⊛ Noise margin



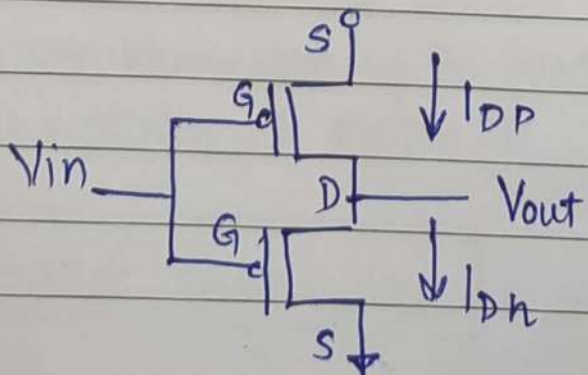


VtH is mid point

⇒ Noise margin is the range which is tolerable to the CMOS such that the output is not impacted. here noise : Voltage
in brief : It is total amount of acceptable V.

$NM_L = V_{IL} - V_{OL}$

V_{DD} is also written, but not equal to V_{OH} because there might be some voltage drop across PMOS.



let the NMOS be operating in saturation region & PMOS in linear region

$$I_{dn} = \frac{1}{2} K_n (V_{GSn} - V_{tn})^2$$

(saturation)
NMOS

$$I_{dp} = K_p \left[(V_{GSp} - V_{to}) \cdot V_{DSp} - \frac{1}{2} V_{DSp}^2 \right]$$

equating both of them

$$I_{dn} = I_{dp}$$

$$\frac{1}{2} K_n [V_{in} - V_{tn}]^2 = K_p \left[(V_{in} - V_{DD} - V_{tp})(V_{out} - V_{DD}) - \frac{1}{2} (V_{out} - V_{DD})^2 \right]$$

Considering for B →

Now we are interested in finding V_{IL}.

diff wrt V_{in}

~~$2 \times \frac{1}{2} K_n (V_{in} - V_{tn})^2 = K_p [$~~

$$K_n (V_{in} - V_{tn}) = K_p \times \left[\left(\frac{dV_{in}}{dV_{in}} - 0 - 0 \right) \times (V_{out} - V_{DD}) + \left(\frac{dV_{out}}{dV_{in}} - 0 \right) \times (V_{in} - V_{DD} - V_{to}) - \frac{1}{2} \times 2 (V_{out} - V_{DD}) \cdot \frac{dV_{out}}{dV_{in}} \right]$$

$$K_n(V_{in}-V_{tn}) = k_p\left[(V_{out}-V_{DD}) + \frac{dV_{out}}{dV_{in}}(V_{in}-V_{DD}) - (V_{out}-V_{DD})\frac{d(V_{out}}{dV_{in}}\right]$$

assuming that $dV_{out}/dV_{in} = -1$ (slope)

$$\frac{K_n}{K_p}(V_{in}-V_{tn}) = \left[V_{out}-V_{dd}-V_{in}+V_{DD}+V_{tp}+V_{out}-V_{dd}\right]$$

$$\frac{K_n}{K_p}(V_{in}-V_{tn}) = \left[2V_{out}-V_{dd}+V_{tp}-V_{in}\right]$$

let $K_n/K_p = K_R$ for simplification

$$K_R V_{in} + V_{in} = 2V_{out} - V_{dd} + V_{tp} + K_R V_{tn}$$

$$V_{in} = \left[\frac{2V_{out} - V_{dd} + V_{tp} + K_R V_{tn}}{1+K_R}\right]$$

as we are calculating from point B.
i.e V_{IL}, $V_{in} = V_{IL}$ so

$$\boxed{V_{IL} = \frac{2V_{out} - V_{dd} + V_{tp} + K_R V_{tn}}{1+K_R}}$$

$K_R = K_p/K_n$, it is in our hands because rest of the params are not controllable.

[$V_{DD} = 1.8$ for 180nm MOS ckts]

we can't actually control V_{DD}. like there isn't much freedom because it is min required.

$$K_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \qquad \left[C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}\right]$$

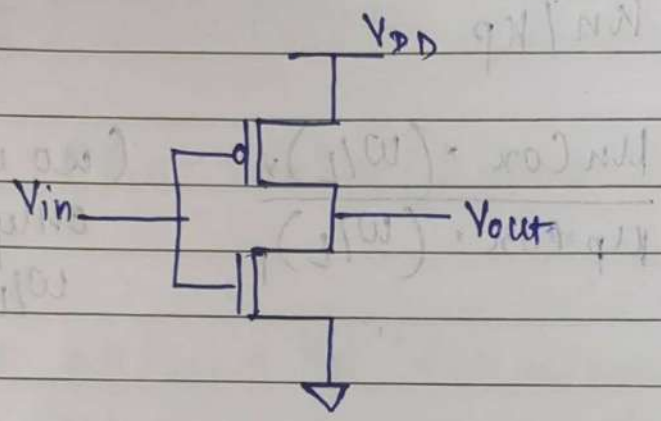
$$K_R = K_n / K_p$$

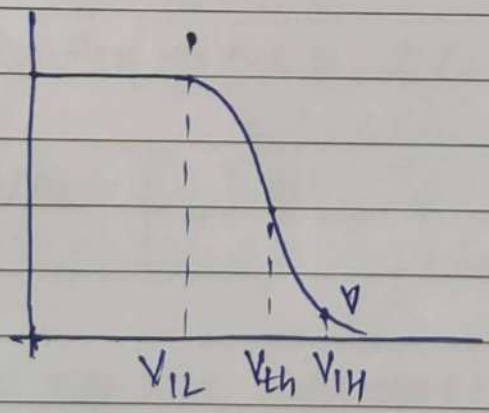
$$K_R = \frac{\mu_n C_{ox} \cdot (W/L)_n}{\mu_p C_{ox} \cdot (W/L)_p}$$

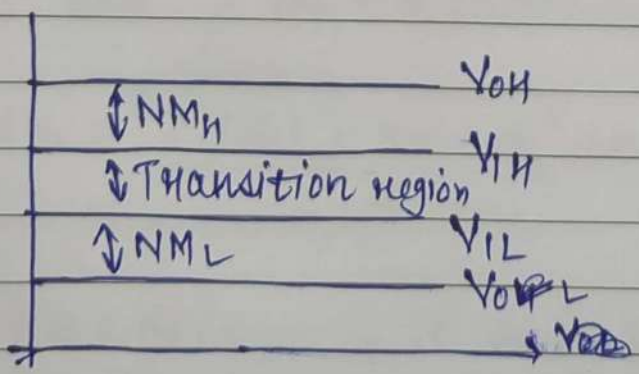
(so we can only control W/L ratio)

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + K_R (2V_{out} + V_{t0,n})}{1 + K_R}$$

$$V_{th} = \frac{V_{t0,n} + \sqrt{\frac{1}{K_R}} (V_{DD} + V_{t0,p})}{1 + \frac{1}{K_R}}$$







V_{IH} is the minimum i/p voltage, which can be interpretet as a logic 1.

V_{IL} is the maximum i/p voltage, which can be interpretet as a logic 0.

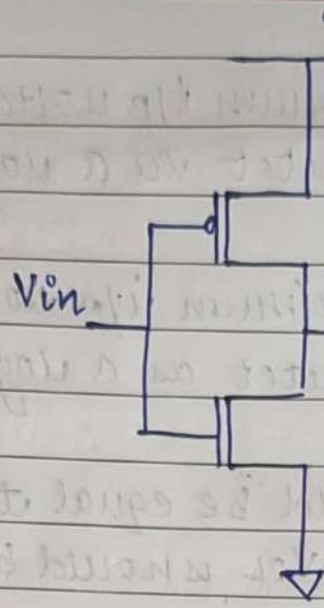
Ideally V_{OH} should be equal to the supply voltage V_{DD}. & V_{OL} should be 0 if there is no drop.

$NM_H = V_{OH} - V_{IH}$ // high noise margin
$NM_L = V_{OL} - V_{IL}$ // low noise margin

If not mentioned then $V_{OH} \approx V_{DD}$
& $V_{OL} \approx GND$

pdf chap 5 : Kang book

TBR: K_n/K_p ratio is almost 2.5 nearly in all cases.



$K_n = 200\mu A/V^2$

$K_p = 80\mu A/V^2$

$$V_{IL} = \frac{2V_{out} + V_{to,p} - V_{DD} + K_R V_{th}}{1 + K_R} \quad \text{—— (1)}$$

$$V_{IH} = \frac{V_{DD} + V_{TO,p} + K_R(2V_{out} + V_{to,n})}{1 + K_R} \quad \text{—— (2)}$$

$$V_{th} = \frac{V_{to,n} + \sqrt{\frac{1}{K_R}}(V_{DD} + V_{to,p})}{1 + \frac{1}{K_R}} \quad \text{—— (3)}$$

$$K_R = \frac{K_n}{K_p} = 2.5$$

putting given data in (I)st formula.

$$V_{IL} = \frac{2\,V_{out} - 0.7 - 3.3 + (2.5)\times 0.6}{1 + 2.5}$$

$$= \frac{2V_{out} - 4.0 + 1.5}{3.5}$$

$$V_{IL} = \frac{2V_{out} - 2.5}{3.5} \Rightarrow \boxed{V_{IL} = 0.57\,V_{out} - 0.71}$$

we know that, for I_L, the PMOS is in linear region & NMOS is in saturation region, also $V_{IL} = V_{in}$, so.

$$\frac{1}{2}K_n[V_{in} - V_{tn}]^2 = K_p\left[(V_{in} - V_{DD} - V_{tp})(V_{out} - V_{DD})\right] - \frac{1}{2}(V_{out} - V_{DD})^2$$

$$\frac{K_n}{K_p}(V_{in} - V_{tn})^2 = \left[(V_{in} - V_{DD} - V_{tp})(V_{out} - V_{DD})\right] - (V_{out} - V_{DD})$$

$$2.5(V_{IL} - 0.6)^2 = 2\times(V_{IL} - 3.3 - (-0.7))\times(V_{out} - 3.3) - (V_{out} - 3.3)^2 \quad \text{—④}$$

putting V_{IL} in Eqn ④

$$\Rightarrow 2.5(0.57\,V_{out} - 0.71 - 0.6)^2$$
$$= \left[2(0.57\,V_{out} - 0.71 - 3.3 + 0.70)(V_{out} - 3.3)\right] - \left[V_{out} - 3.3\right]$$

$$\Rightarrow 2.5(0.57\,V_{out} - 1.31)^2$$
$$= \left[2(0.57\,V_{out} - 3.4)(V_{out} - 3.3)\right] - \left[V_{out} - 3.3\right]^2$$

$$\Rightarrow 0.812\,V_{out}^2 + 4.290 - 3.73\,V_{out}$$
$$= (1.14\,V_{out} - 6.8)(V_{out} - 3.3) - V_{out}^2 - 10.89 + 6.6\,V_{out}$$

$$\Rightarrow 0.812\,V_{out}^2 - 3.73\,V_{out} + 4.290 = 1.414\,V_{out}^2 - 3.76\,V_{out} - 6.8\,V_{out} + 22.4 - V_{out}^2 + 6.6\,V_{out} - 10.89$$

$$\Rightarrow 0.812\,V_{out}^2 - 3.73\,V_{out} + 4.290 = 0.414\,V_{out}^2 + 2.87\,V_{out} - 6.8\,V_{out} - 11.51$$

$$\Rightarrow 0.812\,x^2 - 3.73\,x + 4.29 = 0.414\,x^2 - 3.93\,x - 11.51$$

$$\Rightarrow \boxed{0.67\,V_{out}^2 + 0.05\,V_{out} - 7.22 = 0}$$

$$V_{out}^2 + 0.074\,V_{out} - 10.77$$

$$V_{out} = -\left(\frac{-0.074 \pm \sqrt{(0.074)^2 + 4(10.77)}}{2(10.77)}\right)$$

$$= -\left[\frac{-0.074 \pm \sqrt{5.476 + 43.08}}{21.54}\right]$$

$V_{out} = -3.21$ or 3.14

-3.21 ✗ not acceptable

$\boxed{V_{out} = 3.14}$

$$V_{IL} = 0.57\,V_{out} - 0.71$$

$$\boxed{V_{IL} = 1.07}$$

$$V_{IH} = \frac{V_{DD} + V_{TO,p} + K_R (2V_{out} + V_{to,n})}{1 + K_R}$$

for V_{IH}, NMOS will be in linear & PMOS will be in saturation.

$$V_{IH} = \frac{3.3 + (-0.7) + 2.5 (2V_{out} + 0.6)}{1 + 2.5}$$

$$= \frac{3.3 - 0.7 + 5V_{out} + 1.5}{3.5}$$

$$\boxed{V_{IH} = 1.43 V_{out} + 1.17}$$

Writing drain current equation for both

$$I_{dp} = \frac{1}{2} K_p (V_{GSp} - V_{tp})^2$$

$$I_{dn} = K_n \left[(V_{GSn} - V_{ton})(V_{DSn}) - \frac{1}{2}(V_{DSn})^2 \right]$$

after solving for V_{IH}, we get $\boxed{V_{out} = 0.6}$

$$\boxed{V_{IH} = 2.028}$$

$I = I_0 (e^{V/nV_T} - 1)$

V_T = Thermal Voltage

classmate
Date 31-10-22
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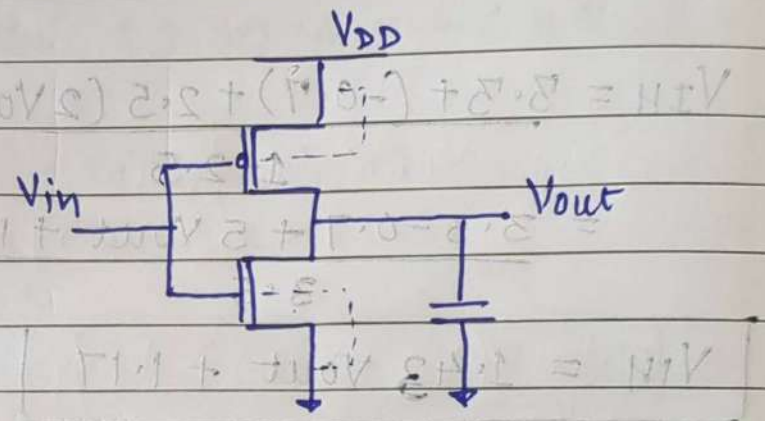
(*) Power dissipation accross CMOS inverter
i) Static power dissipation (P_{dc}) leakage current
ii) dynamic power dissipation (P_{dyn})
iii) Short circuit power loss (P_{sc})



$P_{diss} = P_{dc} + P_{dyn} + P_{sc}$

⇒ We can static power dissipation due to leakage current. $I = I_0(e^{V/nV_T} - 1)$
It is completely unwanted but it is never 0. In terms of eqn, we can write static power as

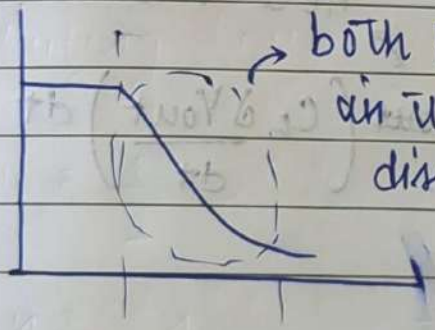
$$P_{dc} = I_0 (e^{V/nV_T} - 1) \times V_{DD}$$

P_{sc} is really really really low. but in VLSI design, there are hell lot of transistors (around a million), so the value of P_{dc} becomes considerable now.

⇒ dynamic power dissipation

when the i/p goes from 0 → 1, the PMOS gets off & NMOS acts as a discharging path & the power is dissipated through it. The dynamic power dissipation is there, due to charging & discharging of capacitor. or to be more precise

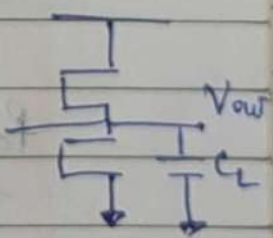
[Pdynamic is due to switching activity]



both PMOS & NMOS are on in this region. & the dissipation here is known as short ckt power loss

Short ckt power dissipation loss is for really less time and at that time both NMOS & PMOS are in ON state & the current gets a direct path to ground.

$$P_{dynamic} = \frac{1}{T}\int_0^T V(t)\cdot i(t)\,dt$$

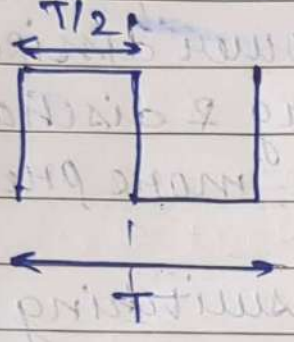


$$P_{dynamic} = \frac{1}{T}\int_0^T V_{out} \times C_L \times \frac{dV}{dt} \times dt$$

$$P_{dynamic} = \frac{1}{T}\int_0^{T/2} V_{out} \times \left(-C_L \times \frac{dV_{out}}{dt}\right) \times dt$$

when charging is done +ve else -ve discharging

why T/2 because half T will be charging & discharging



for charging

here V is accross PMOS so V

$$P_{dynamic} = \frac{1}{T}\int_{T/2}^{T} V_{out}\left(C_L \frac{dV_{out}}{dt}\right) dt \quad = V_{DD} - V_{out}$$

$$P_{dynamic} = \frac{1}{T}\int_{T/2}^{T} (V_{DD} - V_{out})\left(C_L \frac{dV_{out}}{dt}\right) dt$$

Now adding both

$$P_{dyn} = \frac{1}{T} C_L \left[-\int_0^{T/2} V_{out}\, dV_{out} + \int_{T/2}^{T} (V_{DD} - V_{out})\, dV_{out}\right]$$

$$P_{dyn} = \frac{1}{T} \cdot C_L \left[\left[\frac{-V_{out}^2}{2} \right]_0^{T/2} + \left[\frac{2V_{dd} \times V_{out} - V_{out}^2}{2} \right]_{T/2}^{T} \right]$$

$$= \frac{1}{T} C_L \left[\left[\frac{-V_{out}^2}{2} \right]_{0=V_{DD}}^{T/2=0} + V_{dd} \left[V_{out} \right]_{T/2}^{T=V_{DD}} - \left[\frac{V_{out}^2}{2} \right]_{T/2}^{T} \right]$$

$$= \frac{1}{T} \times C_L \left[\frac{-1}{2} \left[-V_{DD}^2 \right] + V_{dd} \times \left[V_{dd} - 0 \right] - \left[\frac{V_{dd}^2}{2} - 0 \right] \right]$$

$$= \frac{1}{T} \times C_L \left[\frac{V_{DD}^2}{2} + V_{dd}^2 - \frac{V_{dd}^2}{2} \right]$$

$$= \frac{1}{T} \times C_L \times V_{dd}^2$$

$$\boxed{P_{dynamic} = \frac{1}{T} \cdot C_L \cdot V_{dd}^2}$$

here T is time period,
so $f = 1/T$ here

$$\left[P_{dynamic} = f \cdot C_L \cdot V_{dd}^2 \right]$$

Now, we can see that, it is still dependent on the switching activity.

f can be depicted as $\alpha_{0 \to 1}$